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Deterministic & low-latency transmision

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White Rabbit Overview

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Hardware and Timing Section European Organization for Nuclear Research, CERN

24 November 2017

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CERN accelerator complex



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Time-triggered distributed system

 Each accelerator consist of hundreds of subsystems



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Time-triggered distributed system

- Each accelerator consist of hundreds of subsystems
- Each subsystem performs time-triggered actions



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Time-triggered distributed system

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- Each subsystem performs time-triggered actions
- All actions are orchestrated by the General Machine Timing:
 - UTC time
 - Actions for next milisecond



ADC, DAC, TDC, Fine Delay Generator, ...

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Time-triggered distributed system

- Each accelerator consist of hundreds of subsystems
- Each subsystem performs time-triggered actions
- All actions are orchestrated by the General Machine Timing:
 - UTC time
 - Actions for next milisecond
- Accelerator control is based on:
 - Accurate device synchronization
 - Deterministic data transmission



ADC, DAC, TDC, Fine Delay Generator, ...

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General Machine Timing renovation – White Rabbit

Decision to renovate in 2008

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- Decision to renovate in 2008
- Stringent requirements

Requirement	Value(s)
Network size:	10km & 2000
Accuracy	sub-ns
Message size	1.2–5 kB
Msgs lost per year	1
Network max latency	1ms
Switch max latency	10µs

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- Name & logo

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Deterministic & low-latency transmision

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- Open & based on standards:
 - Bridged Local Area Network
 - 1 Gbit Ethernet
 - Precision Time Protocol

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- Open & based on standards:
 - Bridged Local Area Network
 - 1 Gbit Ethernet
 - Precision Time Protocol
- Extends standards to meet CERN requirements with two services:
 - Sub-ns synchronization
 - Deterministic and low-latency data transmission
- Foreseen for non-radiation areas (in radiation: WorldFIP – now, Powerlink – in future)

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White Rabbit applications

- Particle accelerators
 - CERN
 - GSI (Germany)
 - JINR Dubna (Russia)

European Organization for Nuclear Research, CERN



All users: www.ohwr.org/projects/white-rabbit/wiki/WRUsers

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White Rabbit applications

- Particle accelerators
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 - JINR Dubna (Russia)
- Cosmic ray & neutrinos detectors
 - LHAASO (China)
 - HiSCORE (Siberia)
 - KM3NET (at the bed of Mediterranean)

The Large High Altitude Air Shower Observation



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National Metrology Institutes

- MIKES (Finland)
- VSL (Netherlands)
- LNE-SYRTE (France)

Finish National Metrology Institute



All users: www.ohwr.org/projects/white-rabbit/wiki/WRUsers

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Open and commercially available off-the-shelf



www.ohwr.org/projects/white-rabbit/wiki/wrcompanies

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Sub-ns synchronization

- Precision Time Protocol (PTP, IEEE1588)
- Layer 1 Syntonization
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model
- Performance
- Standardization



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- Network Latency Contributors
- Latency in WR Switch
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- Using synchronization and determinism
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Sub-ns synchronization

- Synchronization performance:
 - Sub-ns accuracy: max(|TE|) < 1 ns
 - Sub-50 ps precision: sdev(TE) < 50ps



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Sub-ns synchronization

- Synchronization performance:
 - Sub-ns accuracy: max(|TE|) < 1 ns
 - Sub-50 ps precision: sdev(TE) < 50ps
- Building blocks:
 - Precision Time Protocol (PTP, IEEE1588)
 - Layer 1 syntonization
 - Digital Dual Mixer Time Difference
 - Link delay model



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Precision Time Protocol (PTP, IEEE1588)



Packet-based synchronization protocol

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Precision Time Protocol (PTP, IEEE1588)



Packet-based synchronization protocolSimple calculations:

• Link *delay_{ms}*
$$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

• Clock offset_{ms} =
$$t_2 - t_1 + \delta_{ms}$$

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Precision Time Protocol (PTP, IEEE1588)



- Packet-based synchronization protocolSimple calculations:
 - Link *delay_{ms}* $\delta_{ms} = \frac{(t_4 t_1) (t_3 t_2)}{2}$
 - Clock offset_{ms} = $t_2 t_1 + \delta_{ms}$
- Sub-µs synchronisation

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- Packet-based synchronization protocolSimple calculations:
 - Link *delay_{ms}* $\delta_{ms} = \frac{(t_4 t_1) (t_3 t_2)}{2}$
 - Clock offset_{ms} = $t_2 t_1 + \delta_{ms}$
- Sub-µs synchronisation
- Limitations:
 - Free-running oscillators
 - Timestamping precision
 - Medium asymmetry

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Layer 1 Syntonization

- All network devices use the same physical layer clock
- Clock is encoded in data by master and recovered by slave
- Clock loopback and phase detection allow precise timestamps



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Digital Dual Mixer Time Difference (DDMTD)

- Clever implementation of a phase detector in an FPGA
- Uses D-flip-flops to zoom-in phase offset
- Allows for phase measurements at picosecond level



www.cern.ch/white-rabbit/documents/DDMTD_for_Sub-ns_Synchronization.pdf

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Link delay model

Hardware delays:

Link asymmetry:



www.cern.ch/white-rabbit/documents/WR_Calibration-v1.1-20151109.pdf

Link delay model

- Hardware delays:
 - Calibrate static delays: Δ_{TXM} , Δ_{RXM} , Δ_{TXS} , Δ_{RXS}
 - Measure semi-static delays: ϵ_M , ϵ_S
- Link asymmetry:



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Link delay model

- Hardware delays:
 - Calibrate static delays: Δ_{TXM} , Δ_{RXM} , Δ_{TXS} , Δ_{RXS}
 - Measure semi-static delays: *ϵ_M*, *ϵ_S*
- Link asymmetry:
 - Single fibre for two-way communication
 - Fibre asymmetry coefficient: $\alpha = \frac{\delta_{MS} \delta_{SM}}{\delta_{SM}}$



www.cern.ch/white-rabbit/documents/WR_Calibration-v1.1-20151109.pdf
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WR Synchronization performance



www.cern.ch/white-rabbit/documents/White_Rabbit-a_PTP_application_for_ robust_sub-nanosecond_synchronization.pdf

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WR standardization in IEEE1588



IEEE standards are revised periodically

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- IEEE standards are revised periodically
- The IEEE1588 is revised by industry/academia

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- IEEE standards are revised periodically
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 - Inclusion of the generalizations



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- Revised IEEE1588 expected in 2018/2019



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Determinism and network latency

Determinism

A deterministic system is predictable: it provides calculable and consistent characteristics of operation that are required by the application, e.g. network latency of data transmission.

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Network latency



Deterministic network is a network in which we can calculate the maximum latency

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Network latency contributors



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Network latency contributors



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Network latency contributors

- Cables: 5us/km we cannot do much about this
- Switch operation We can do something about this
- Other traffic



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Switch in a nutshell



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 - Experimental



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- And what on Earth are priorities...?



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Priorities - standard extension of Ethernet Frame



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WR Switch Not Using priorities



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WR Switch Using Standard Priorities



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WR Switch Using Standard Priorities



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High Priority



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Latency of WR Switch for Fast Forward



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Latency of WR Switch for High Priority



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Open source (H/W & S/W) with commercial availability & support

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 - White Rabbit solutions to be part of IEEE1588 (PTP) standard
 - Compatible enhancement of IEEE802.1Q, similar mechanism in TSN

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- WR Switch and so WR Network
 - Deterministic by (open) design
 - Latency-optimized for selected traffic
 - Upper-bound latency for HP traffic (experimental)

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- Future plans
 - Mechanisms to increase reliability (http://cds.cern.ch/record/2261452)
 - 10 Gbit Ethernet

Thank you



Thank you !

www.cern.ch/white-rabbit



Extras

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Digital Dual Mixer Time Difference (DDMTD)

- Used for precise phase measurements
- Implemented in FPGA and SoftPLL
- 62.5MHz WR clock and N=14 results in 3.814kHz output signals











WR Node IP Core



www.ohwr.org/projects/white-rabbit/wiki/node

WR Node Reference Design for Hardware



www.ohwr.org/projects/white-rabbit/wiki/ wrreferencedesign









WR Reference Network



Performance of the Reference Network

Name	Requirement	In the reference WR network
Network size:	10 km & 2000 nodes	10 km & 2160 nodes
Synchronization :		
- accuracy over a year:	sub-ns	0.41 <i>ns</i>
 accuracy in transient: 	sub-ns	1.19 <i>ns</i>
- precision:	sub-50 ps	31 <i>ps</i>
Control message		
- allowed size	1200–6000 bytes	1200–6000 bytes
- max lost per year	1	1 with probability R(t)
Upper-bound network	< 500 μ <i>s</i>	\leq 78 μ s for network
latency	(derived from 1 ms)	\leq 150 μ s for control message
		0.9854 for $MTBF_{switch} = 40\ 000\ h$
Total reliability $R(t)$	\geq 0.98	0.9967 for <i>MTBF_{switch}</i> = 100 000 <i>h</i>
		0.9997 for <i>MTBF_{switch}</i> = 650 000 <i>h</i>