PPSi – A Free Software PTP Implementation

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Outline

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White Rabbit extension to PTP

- Next-generation CERN control and timing

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- Open Hardware and Open Software
- PTP extension defined as a Profile
- Synchronization:
  - **sub-nanosecond accuracy**
  - **tens of picoseconds precision**

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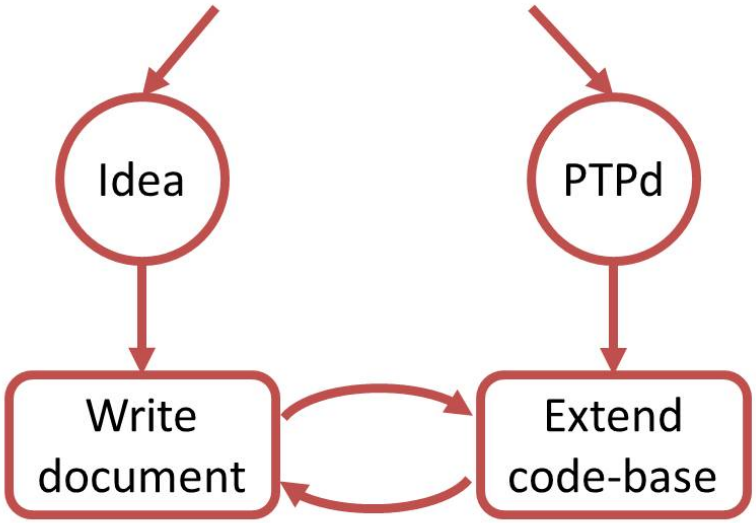

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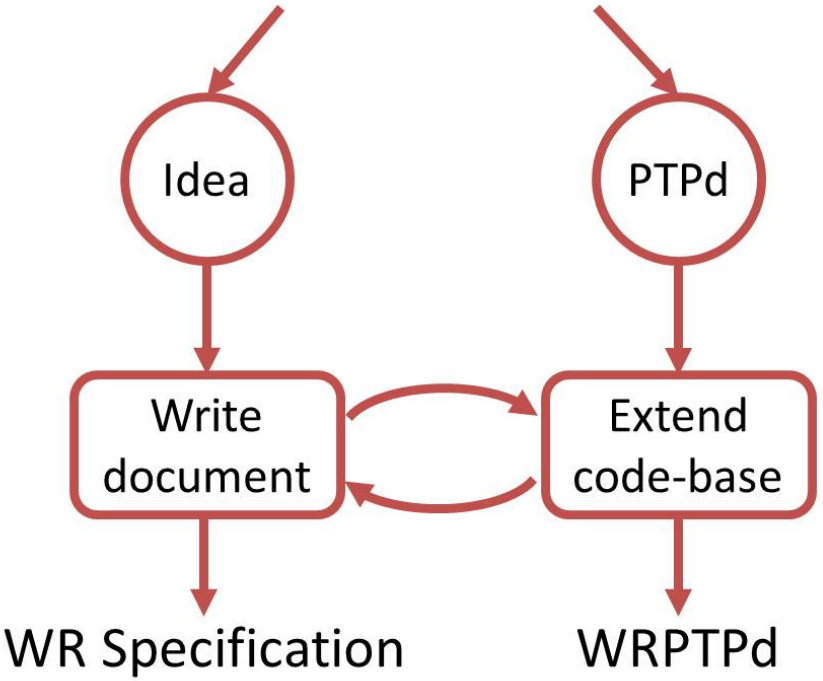


White Rabbit Specification:
Draft for Comments

July 2011

- Unix
- Embedded Linux
- Soft-core in FPGA

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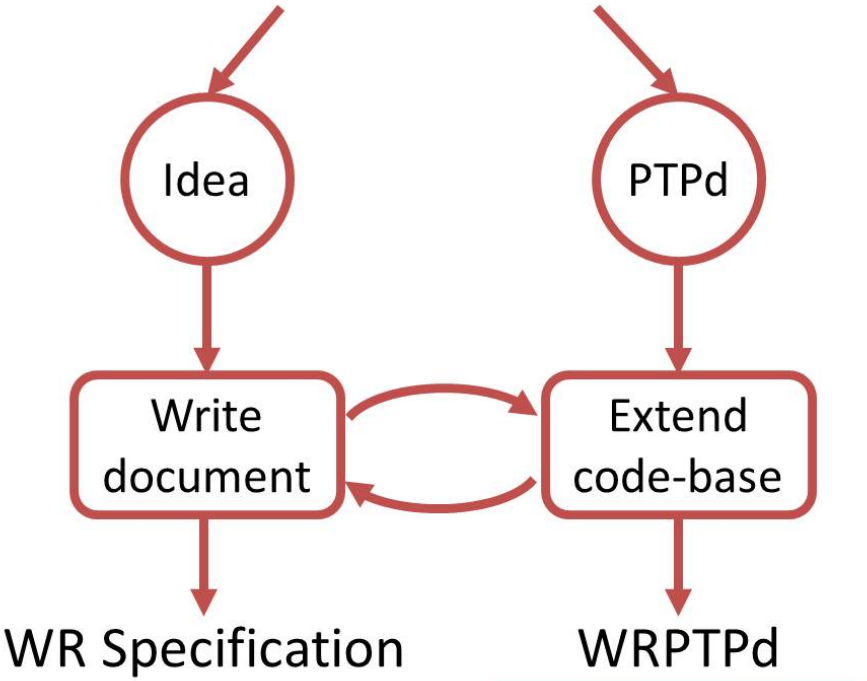


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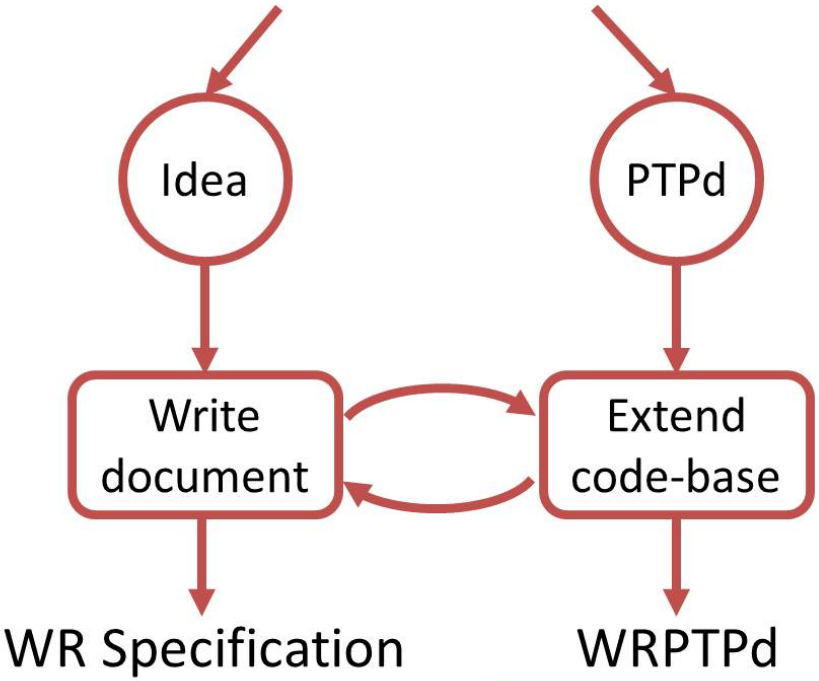

Maintain and debug endlessly

Redesign !!!

PTP Ported To Silicon (PPSi)

- Portable
- Modular
- Extensible
- Free software

PTP Ported To Silicon (PPSi)

- Portable
- Modular
- Extensible
- Free software
- Maintainable
- Beautiful code
- Easy to debug

In short ...

A well-designed and well-coded application that we are proud of.

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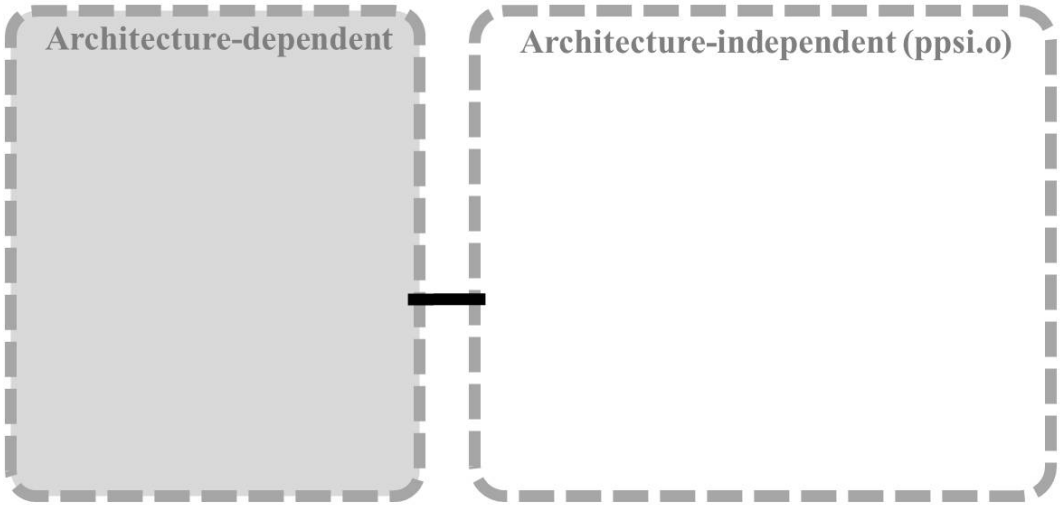
PPSi design overview

- Arch-independent
- Arch-dependent



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  - non-blocking execution
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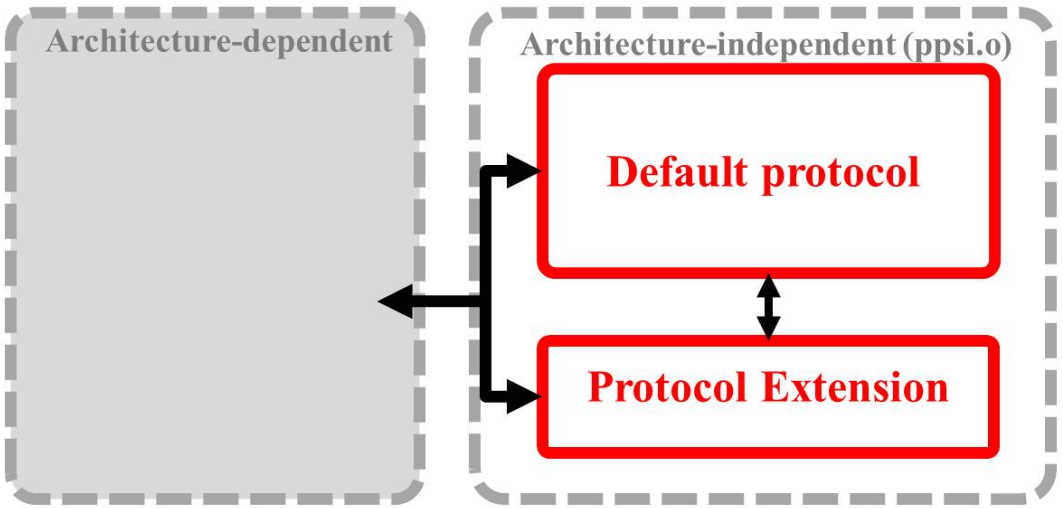

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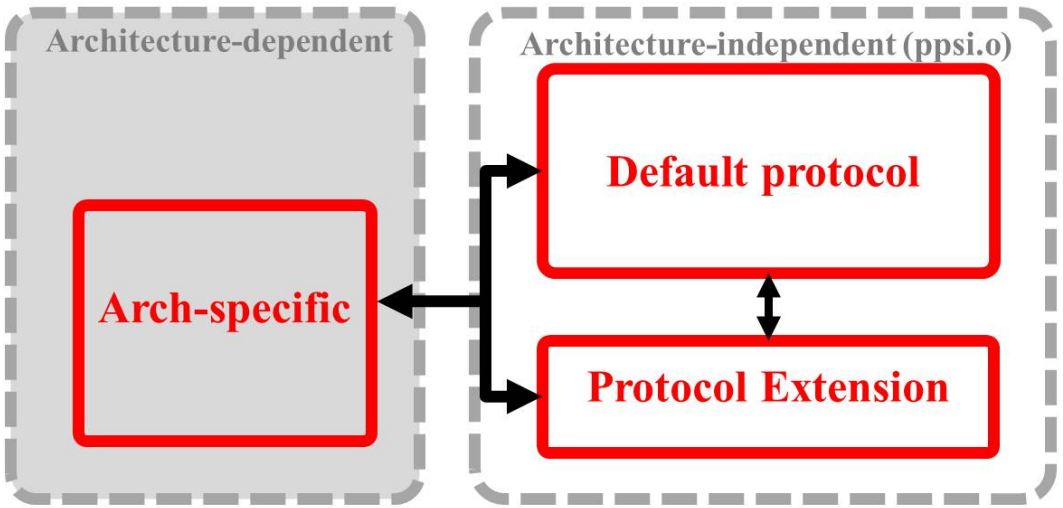

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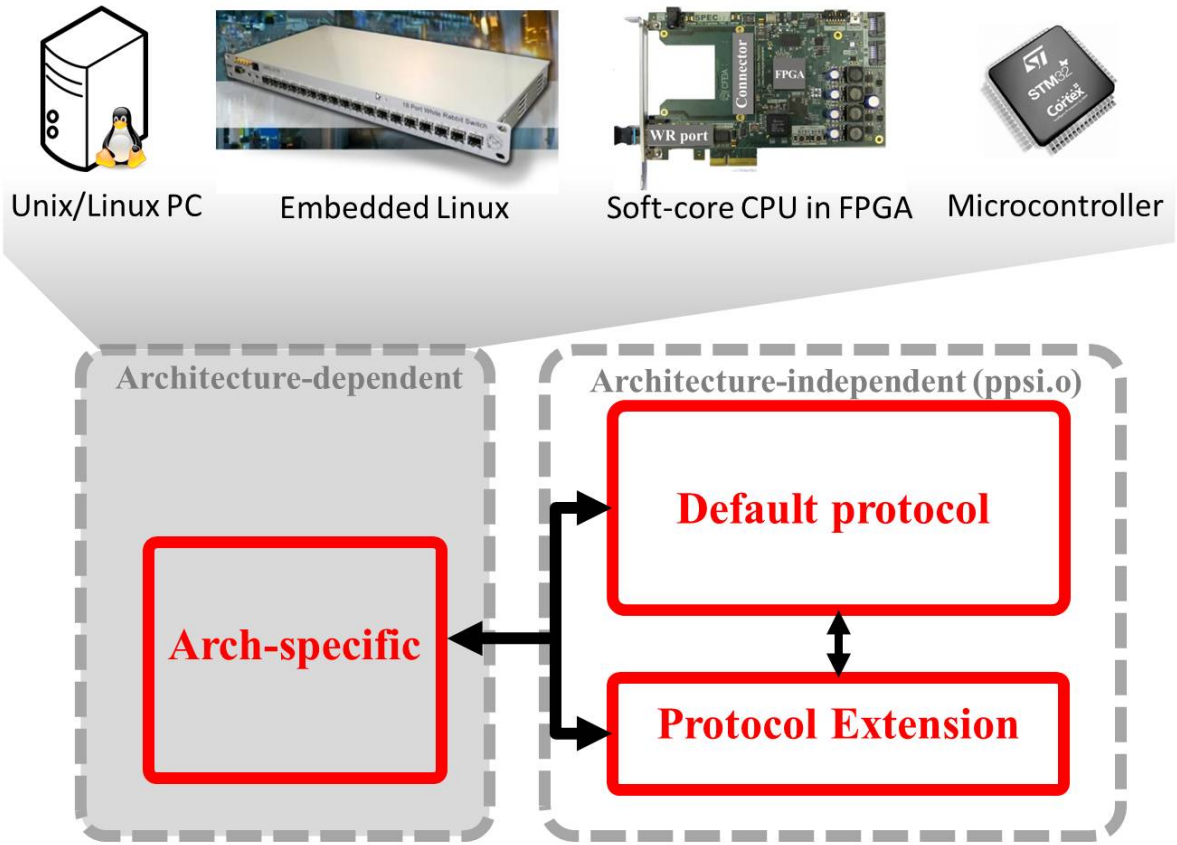

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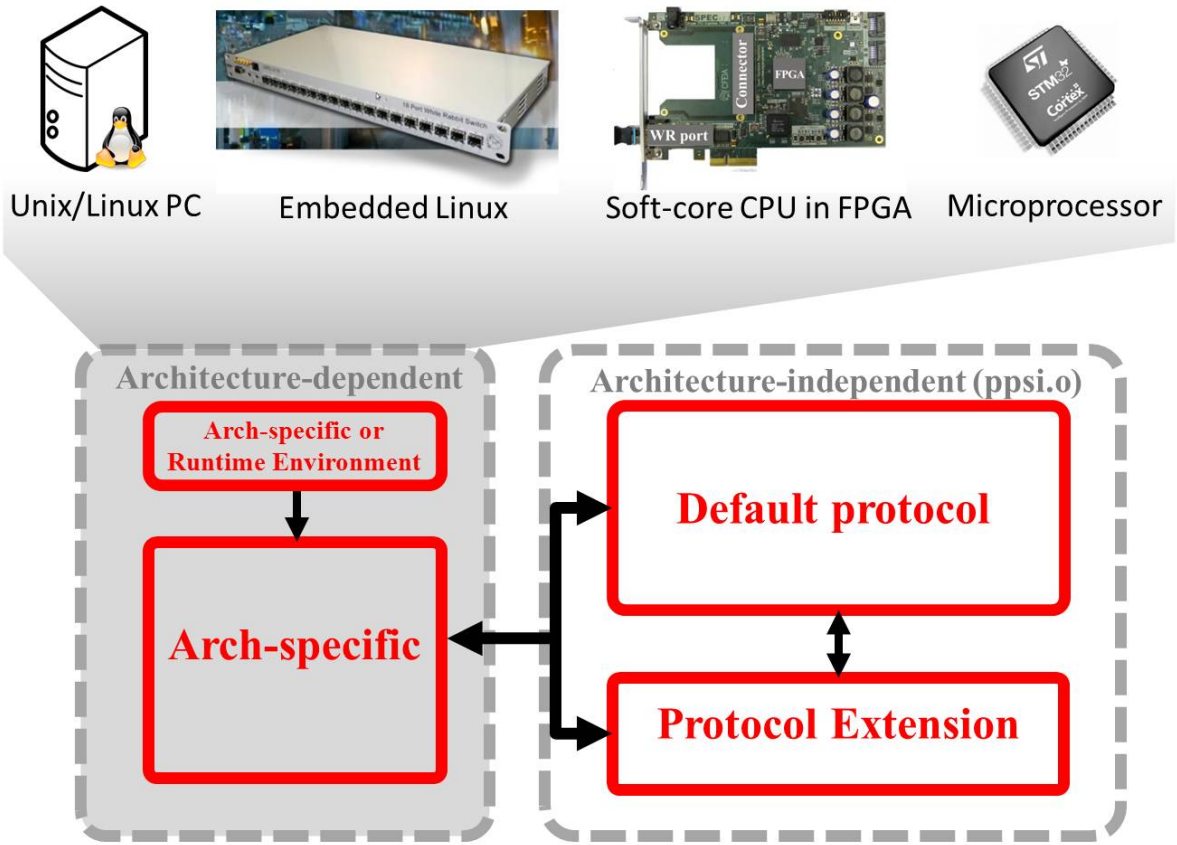

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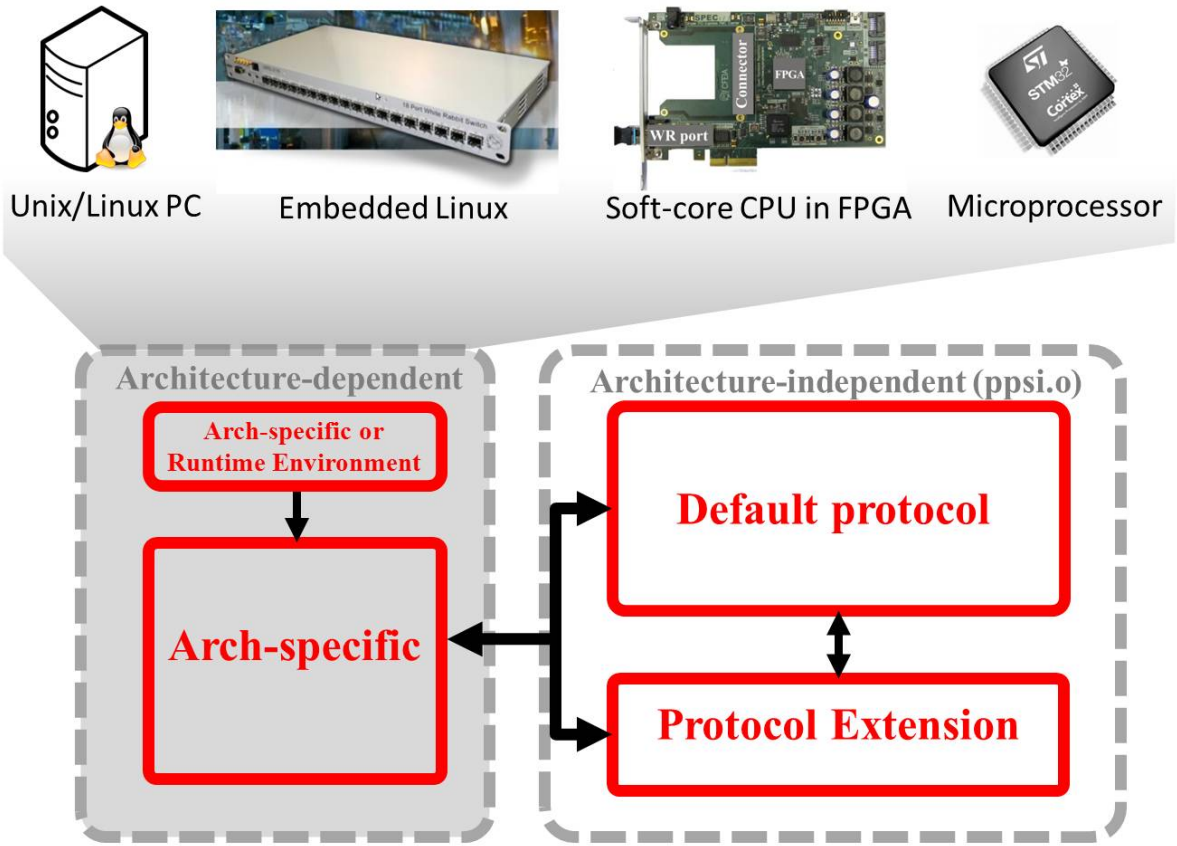
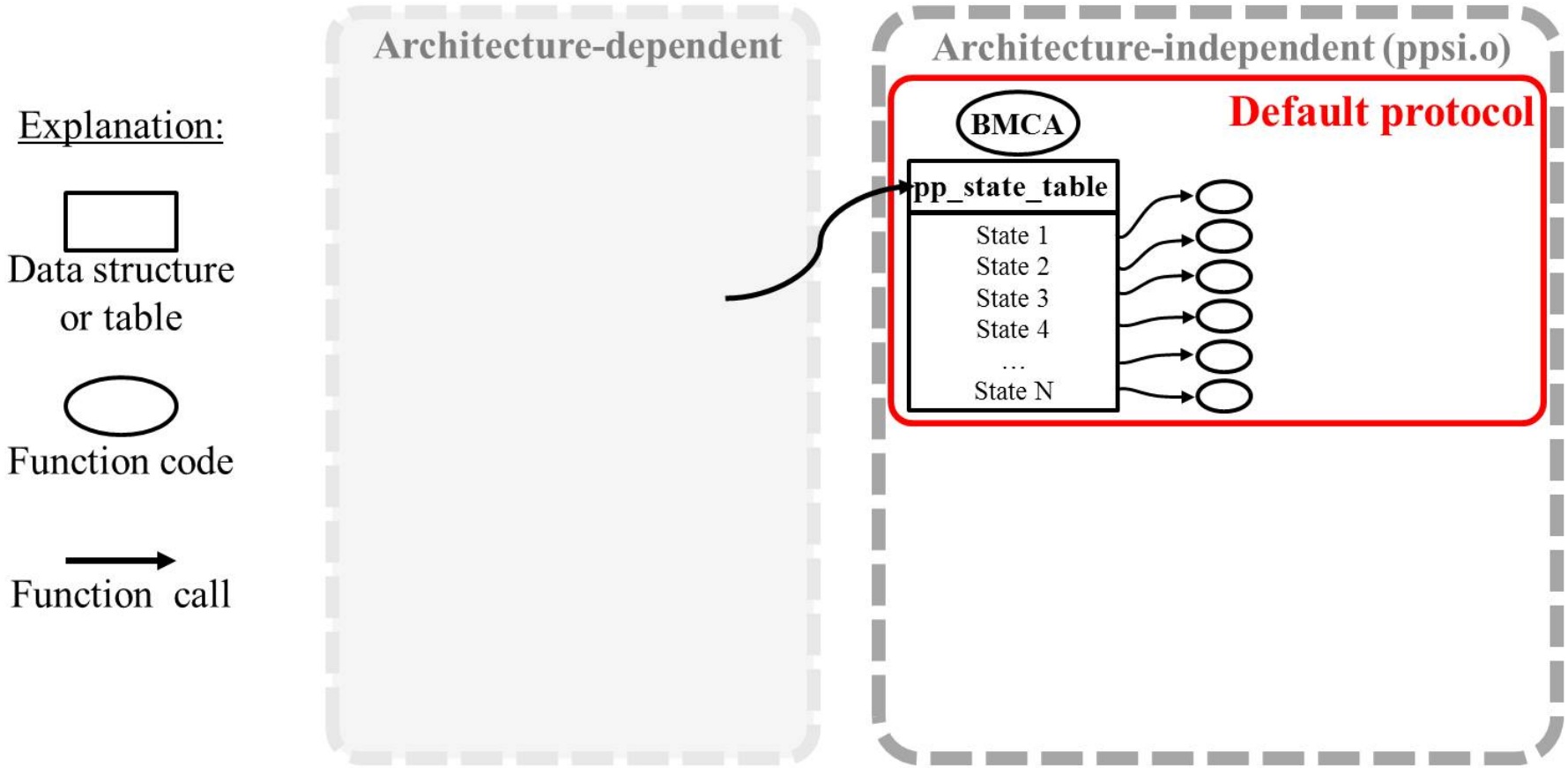


Reflect the PTP layered approach

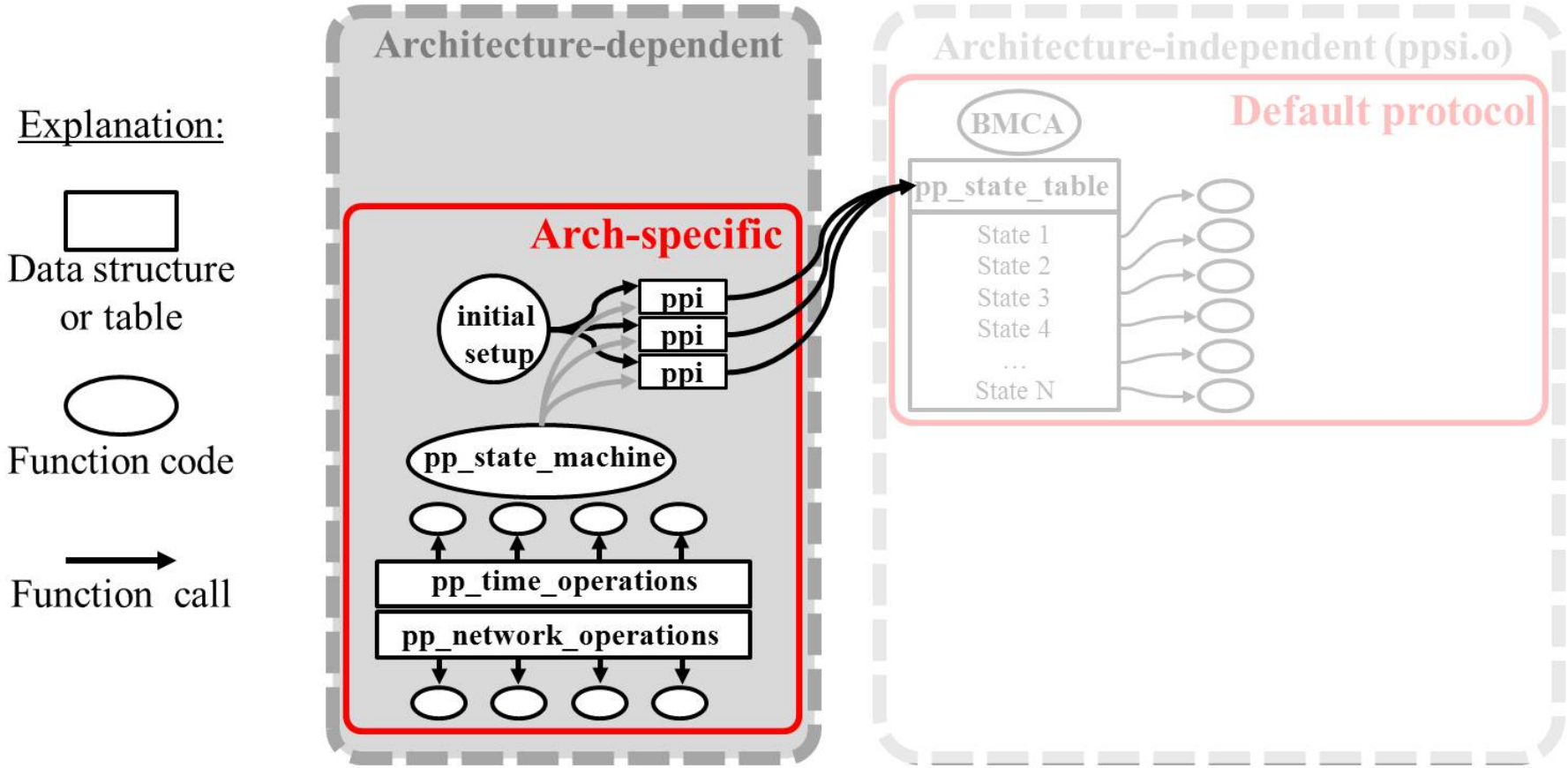
Default protocol code - shared by all architectures

- **Implements**: BMCA, message handling, state machine
- **Executes**: immediately, message– or timeout–triggered
- **Returns**: re-entry delay



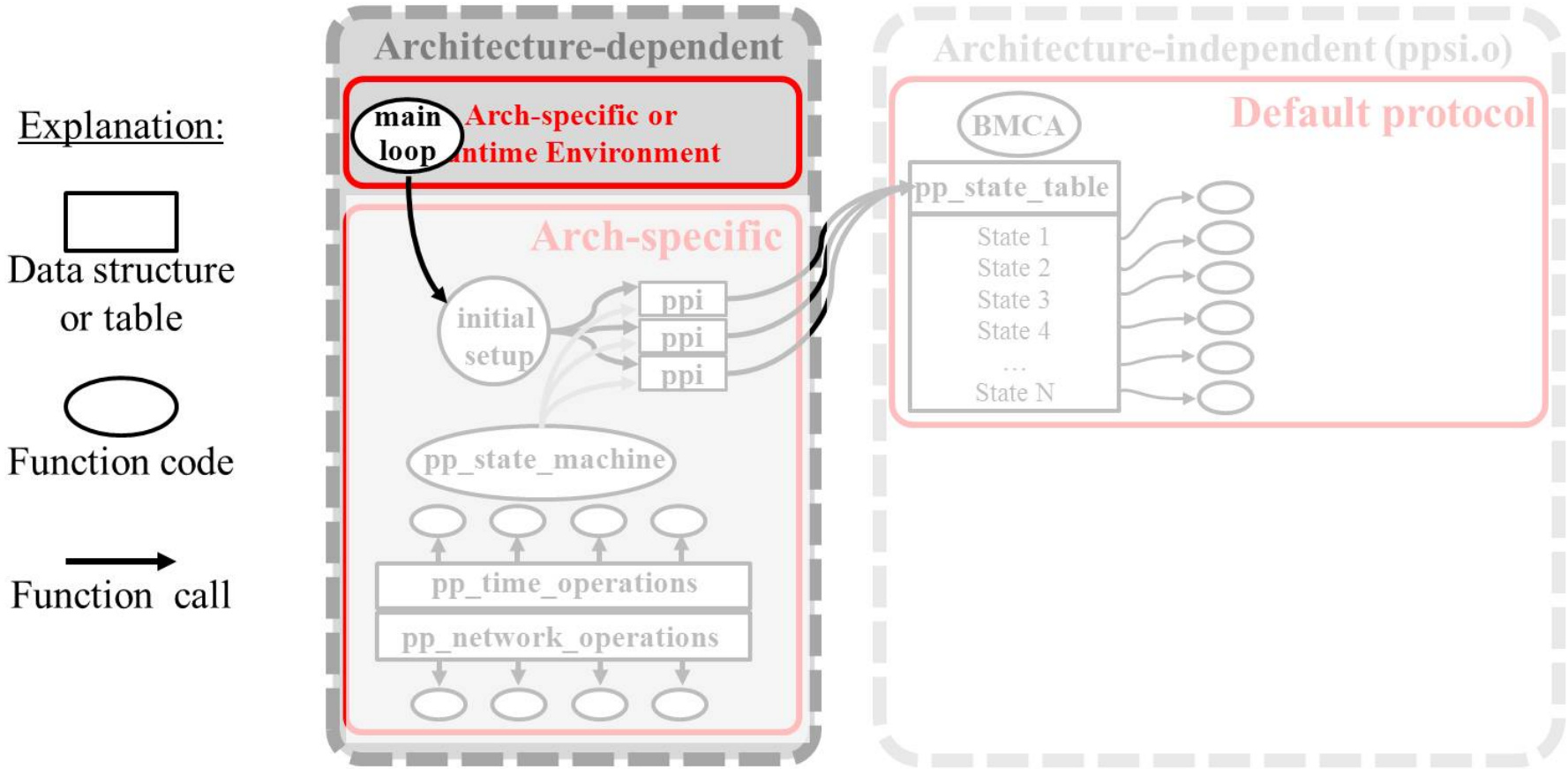
System architecture specific code

- **PPSi instance ppi**: per-port config & runtime data
- **Network operations**: arch– & mapping–specific functions
- **Time operations**: arch– & hardware–specific functions



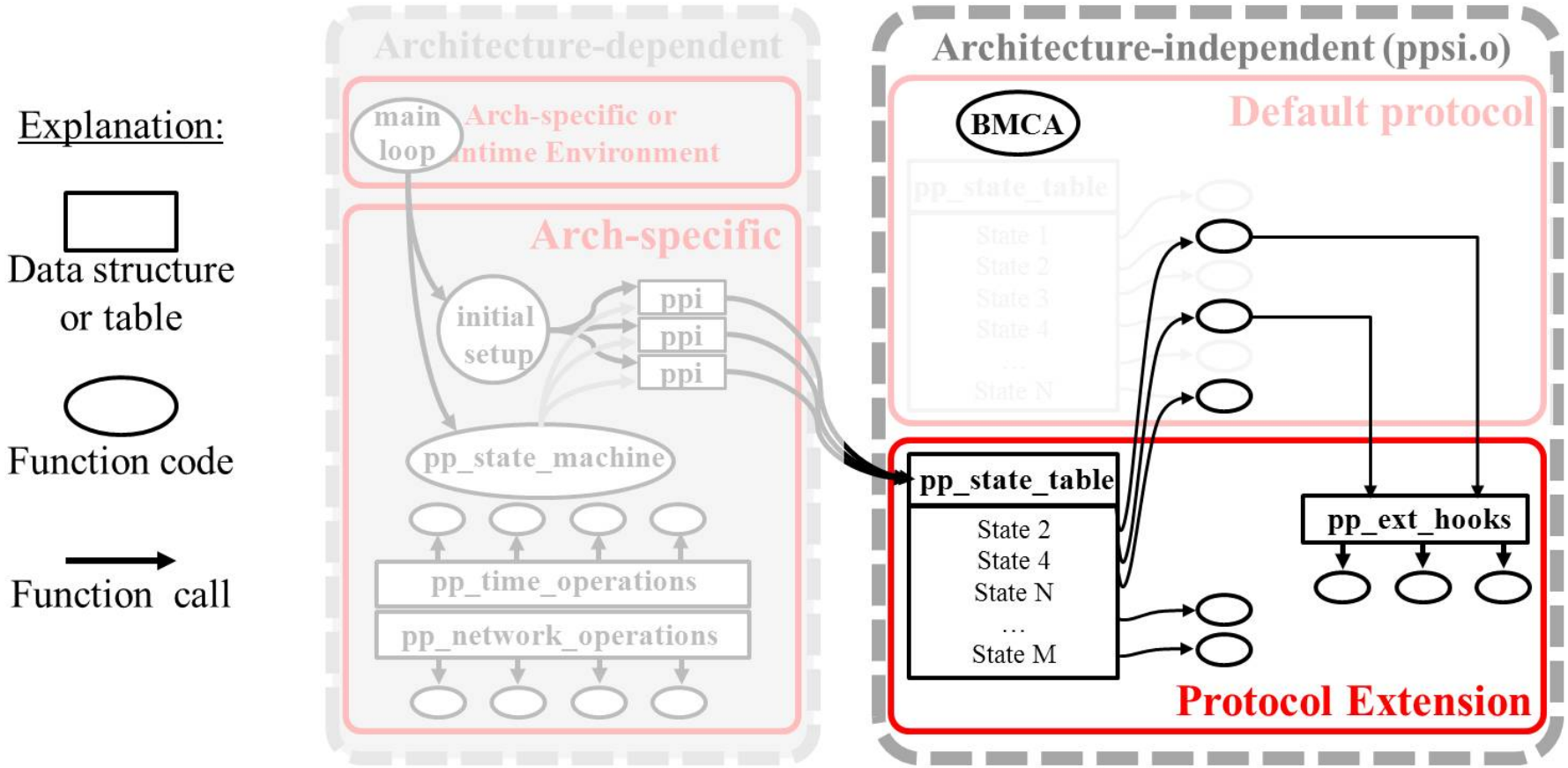
Runtime environment specific code

- **Hosted environment**: main loop of daemon, library access
- **Freestanding environment**: no main function & no library, real-time loop, library-like usage



Extension specific code

- **Defines** custom states
- **Redefines** table with calls to default & custom states
- **Defines** hooks in default protocol code



Portability: supported “arch”

- arch–unix
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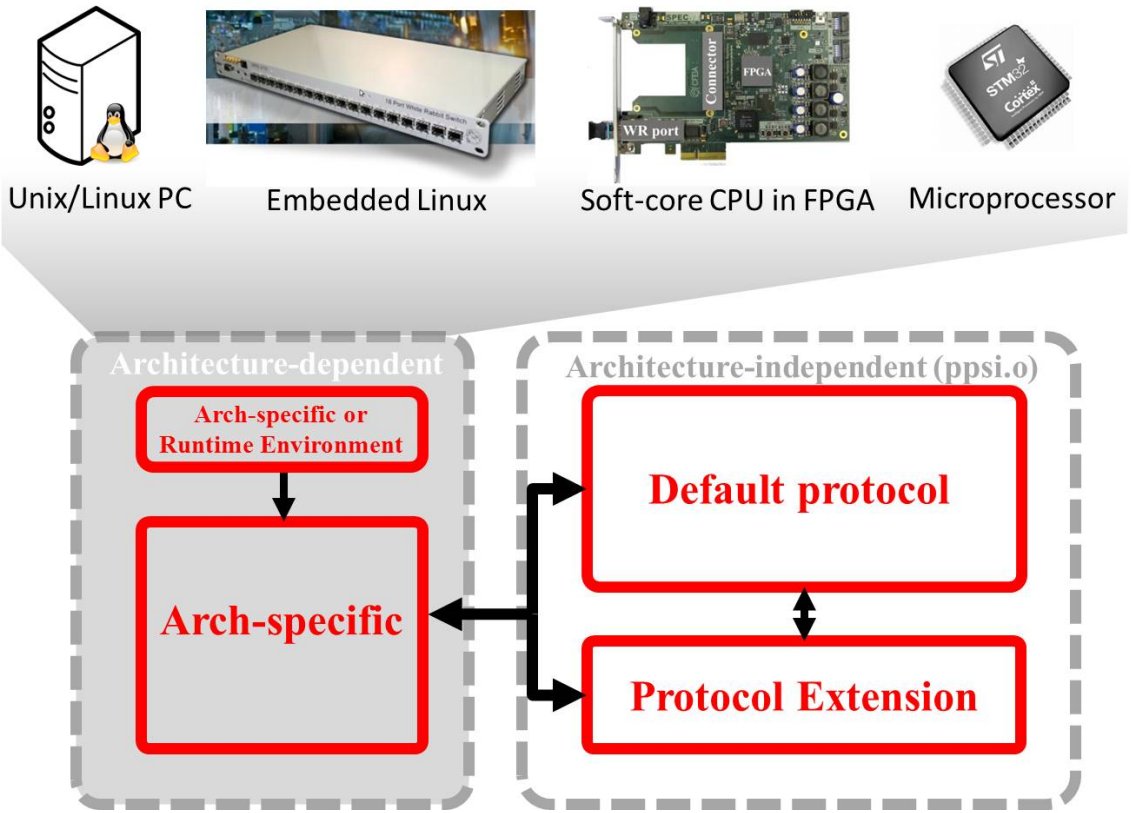

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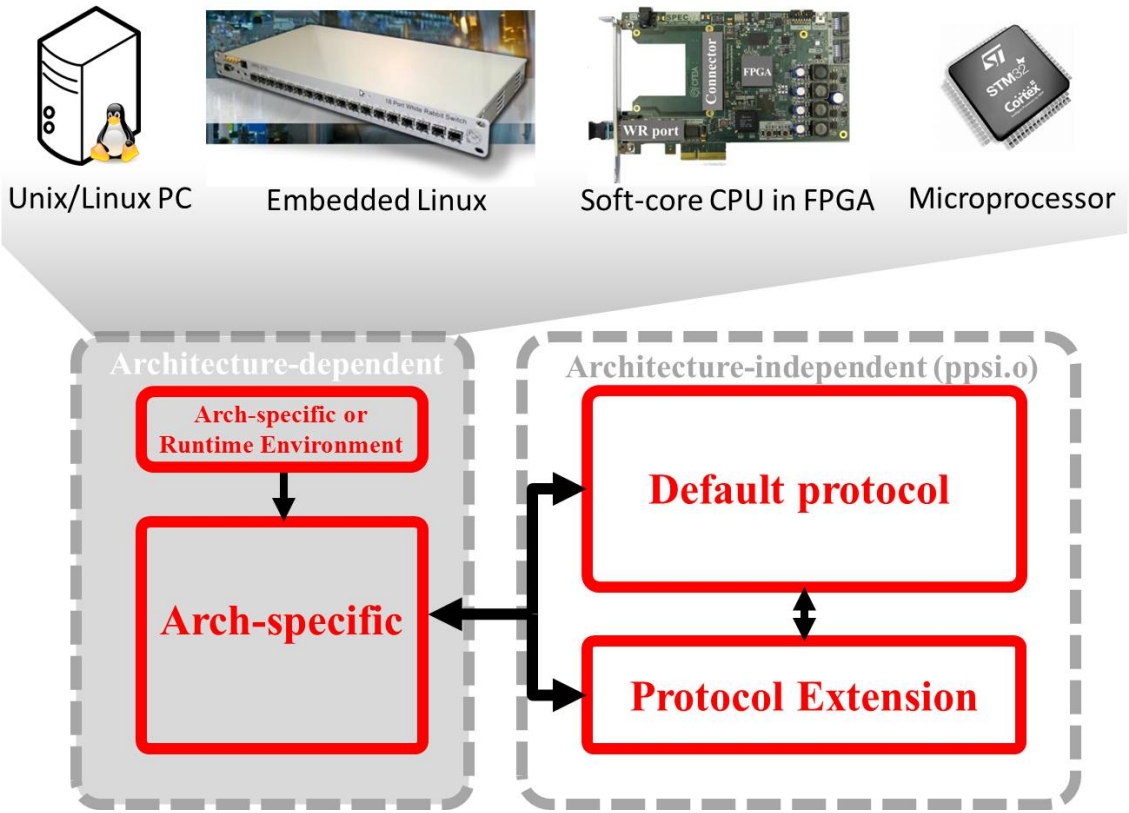

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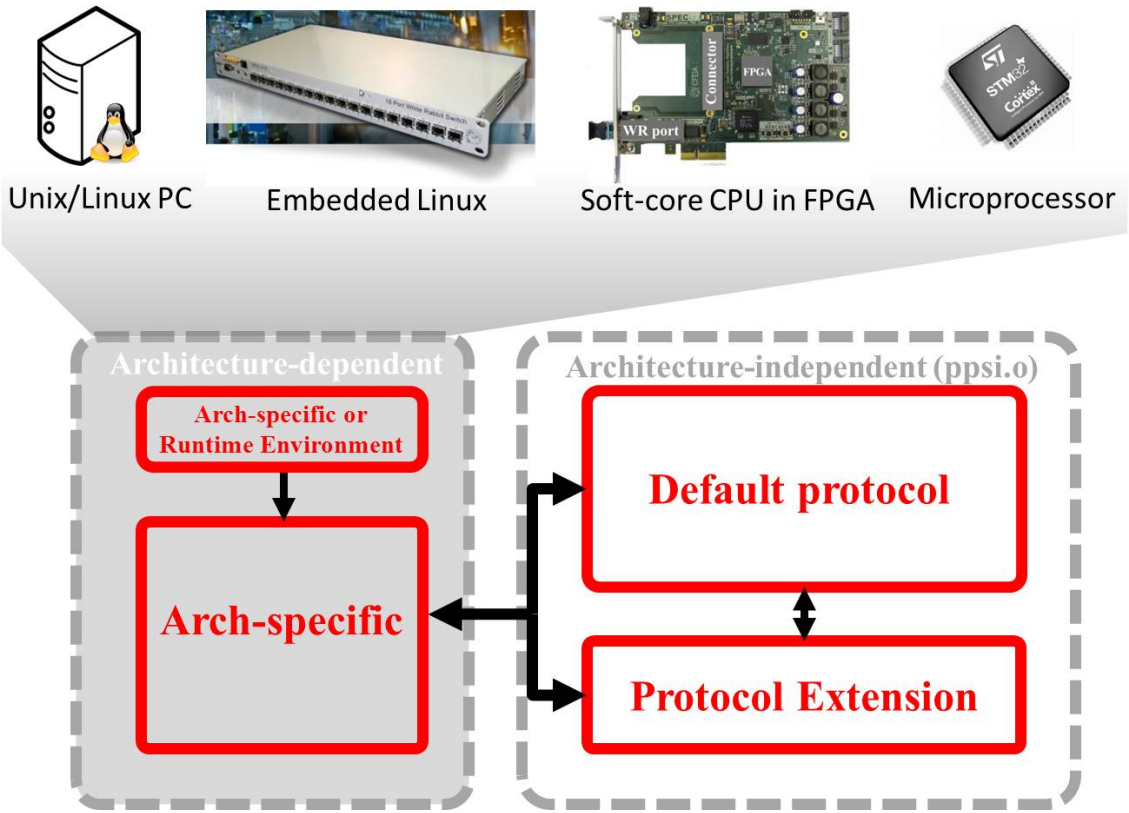

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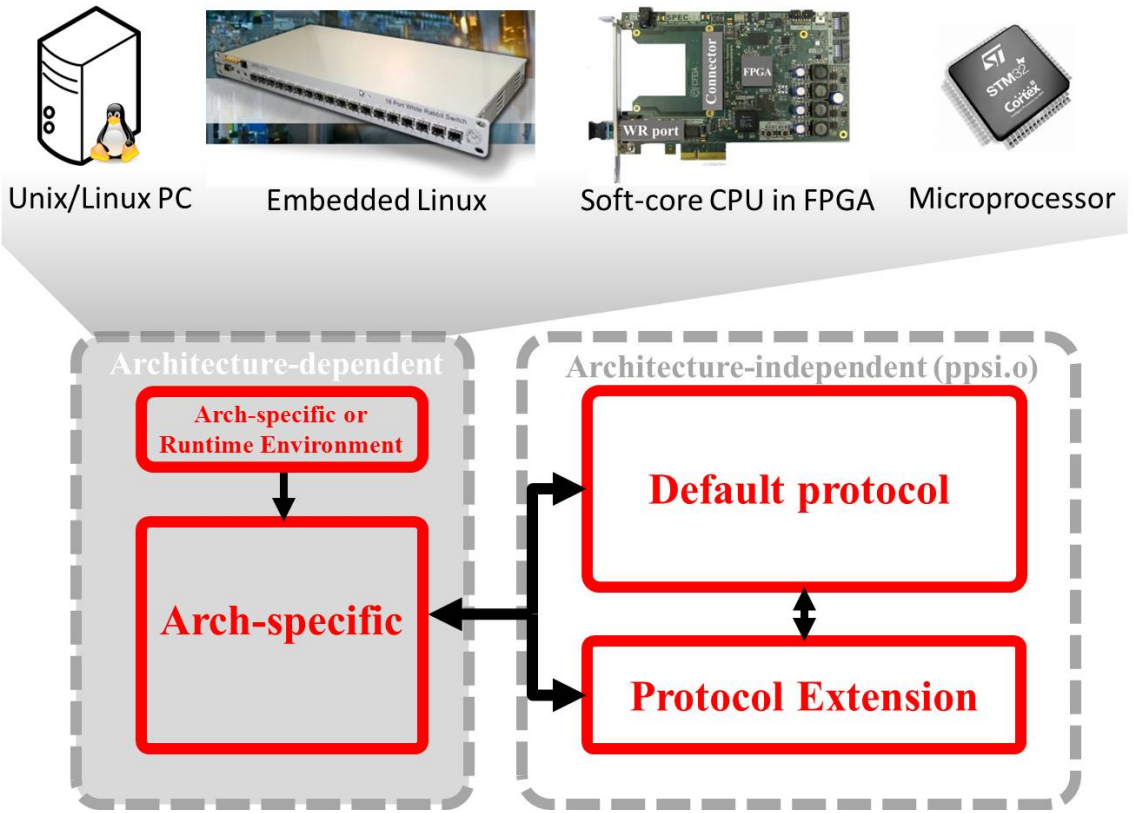

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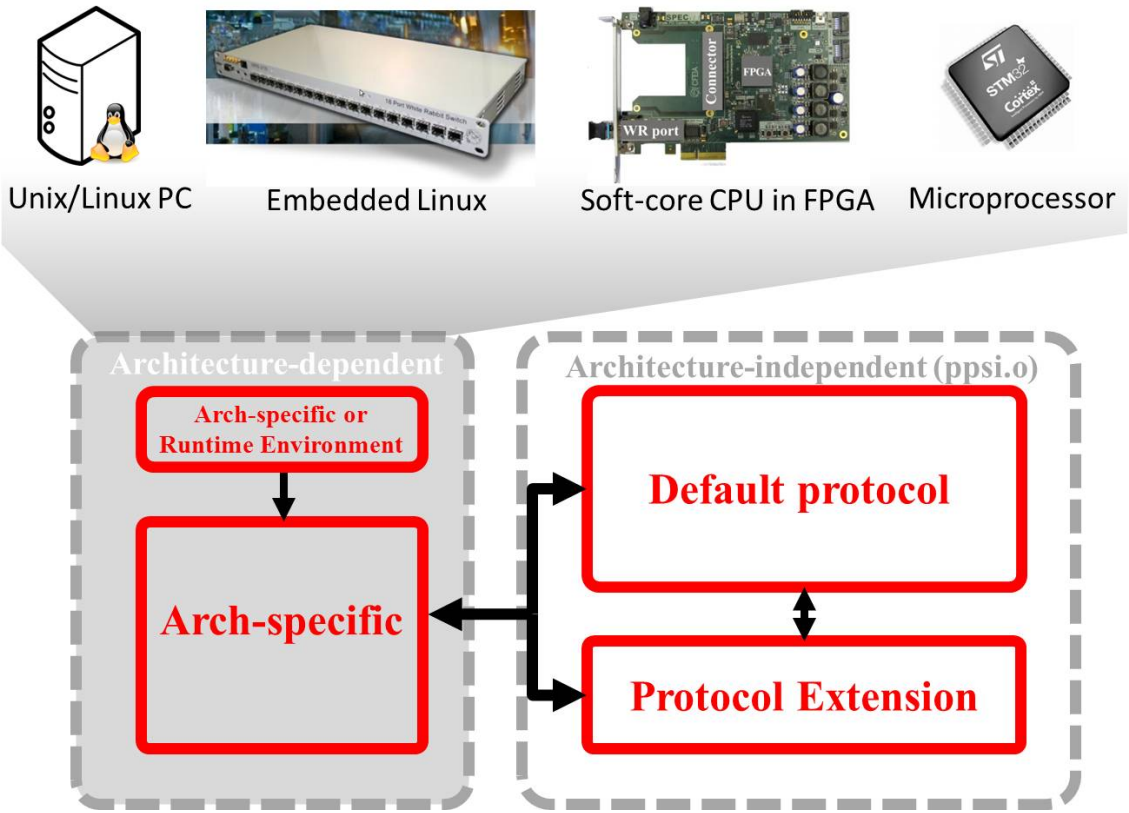

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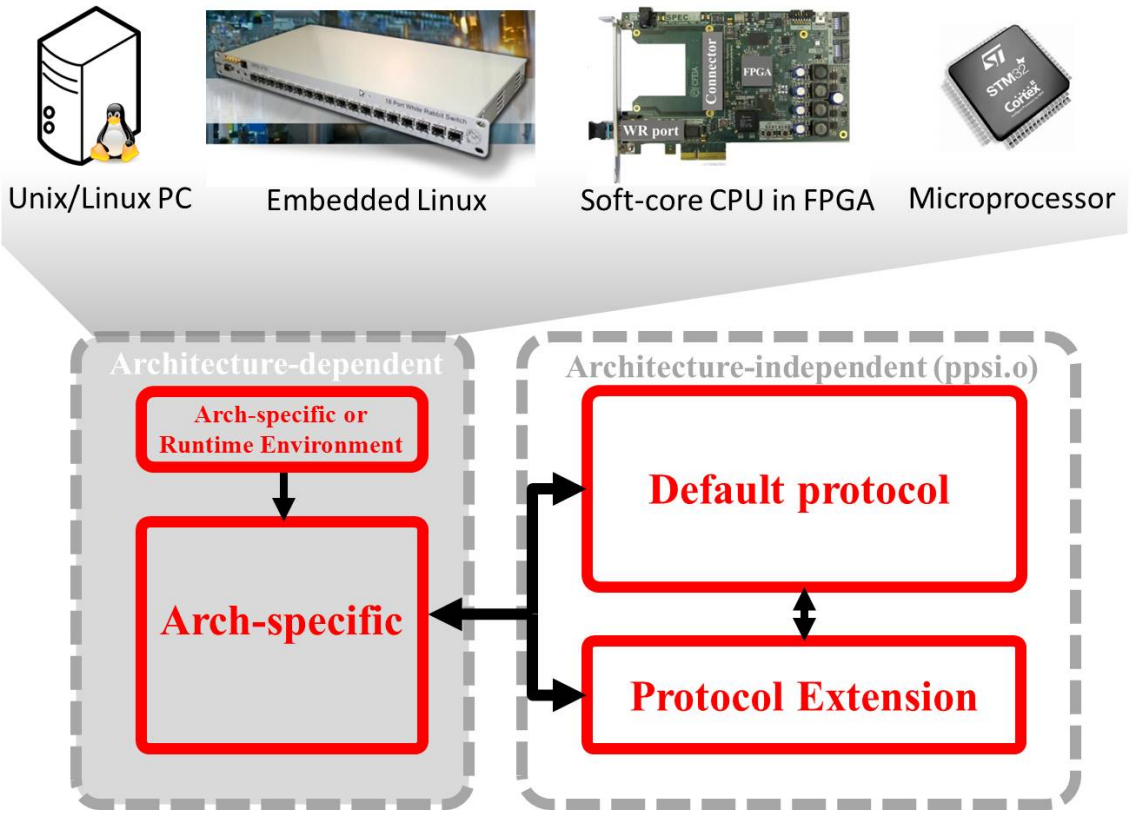
- arch-sim
  - hosted on single Unix PC
  - simulation of two nodes



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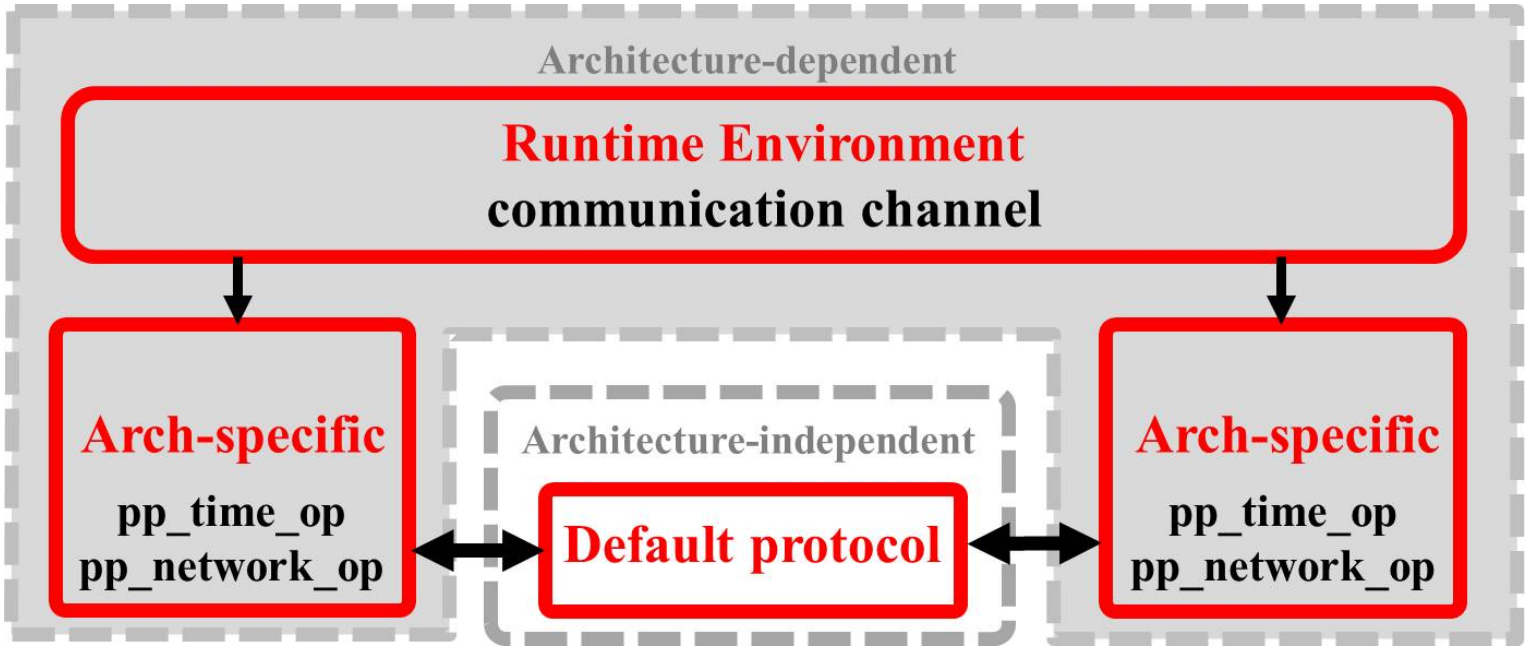

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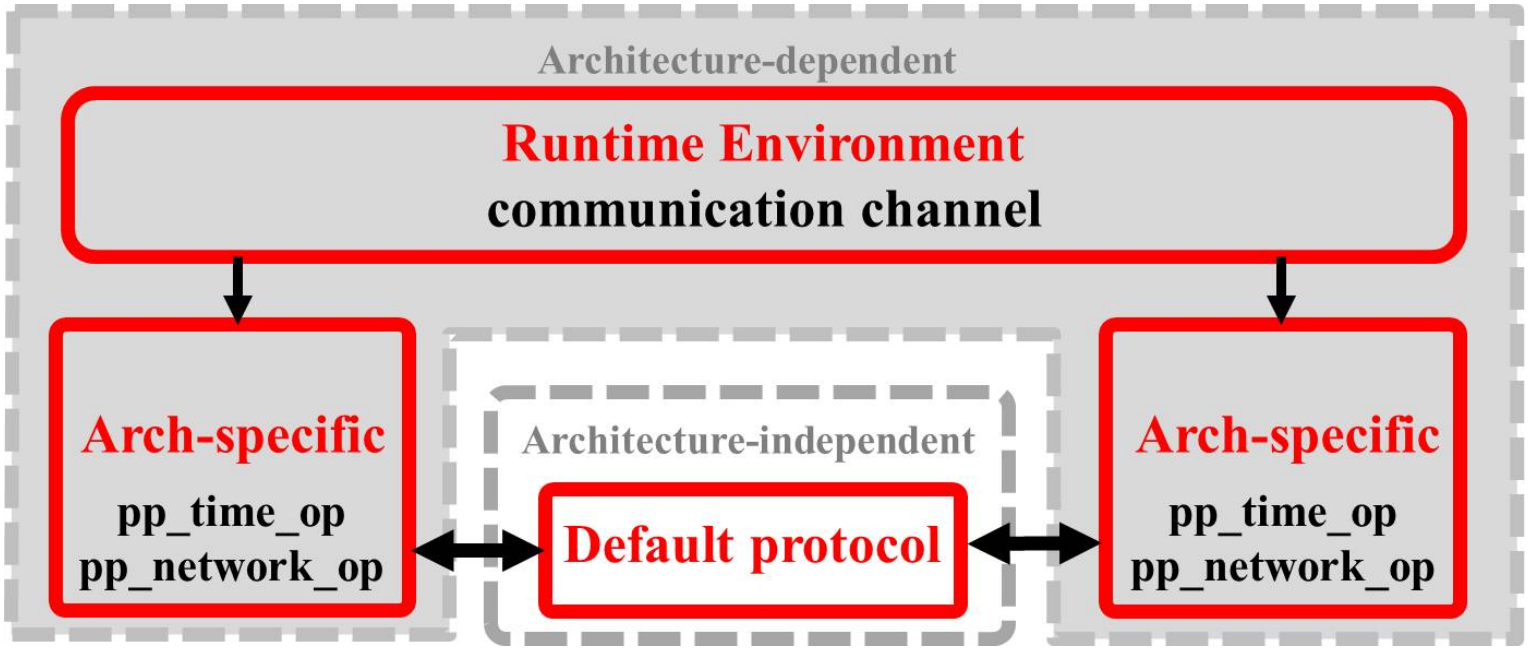

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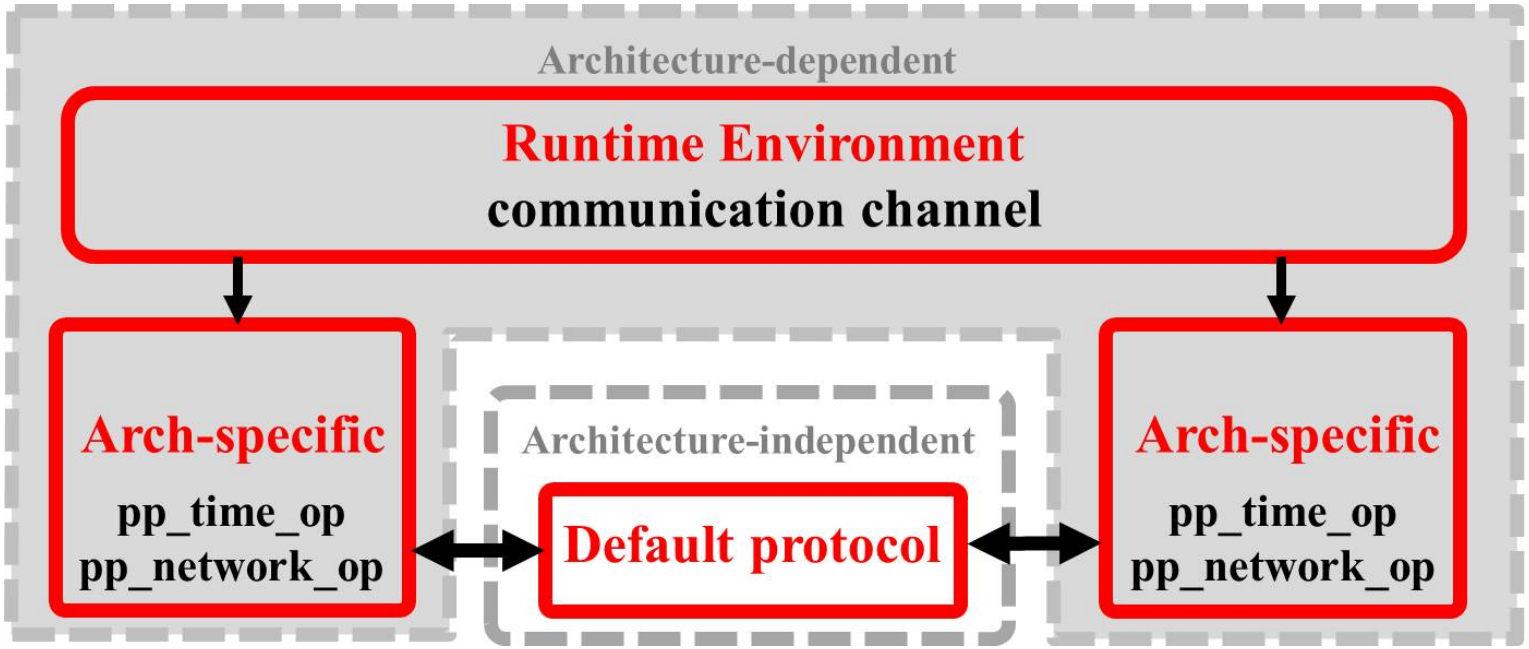

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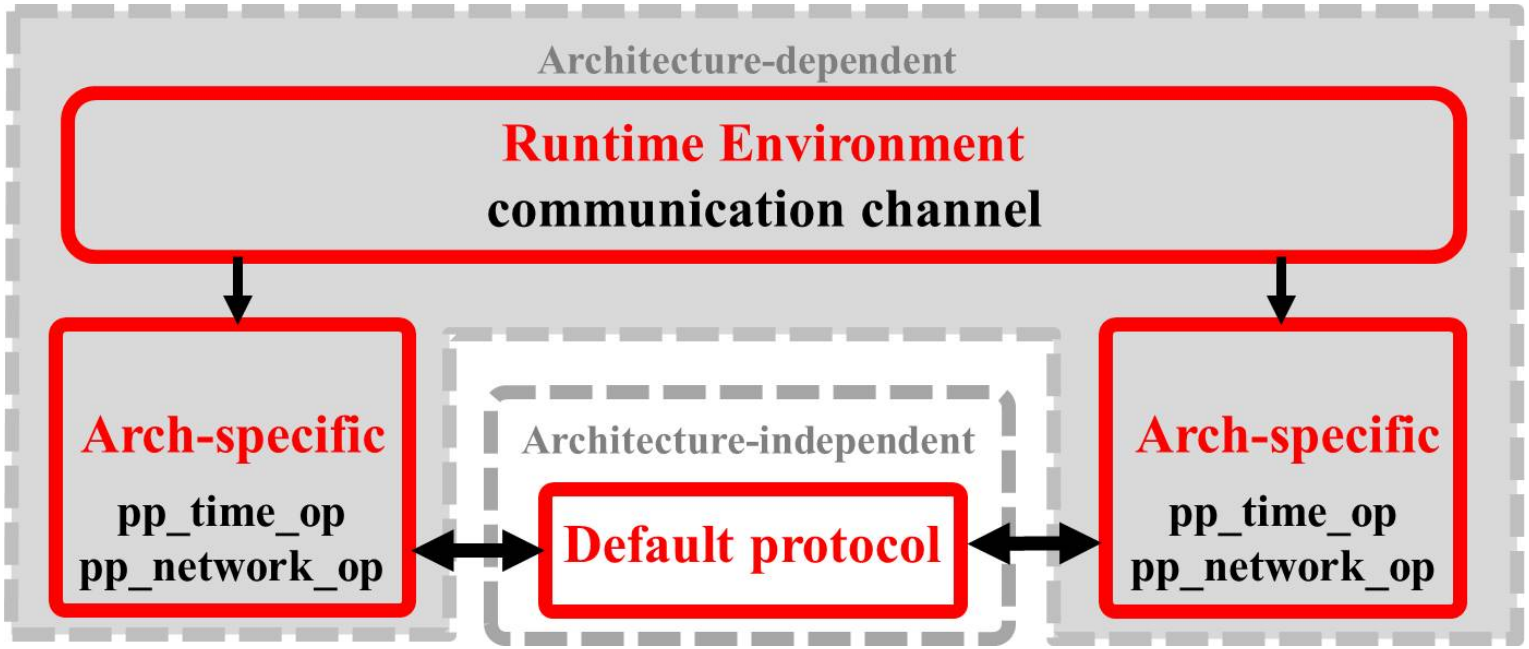

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- Provides time fast-forward benefiting
  - network– & timeout–driven protocol core
  - synchronous & immediate execution of state machine
- Simulates thousands of PTP iterations per second

Simulation to tune and debug non-WR servo

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- Range of packet delay variation
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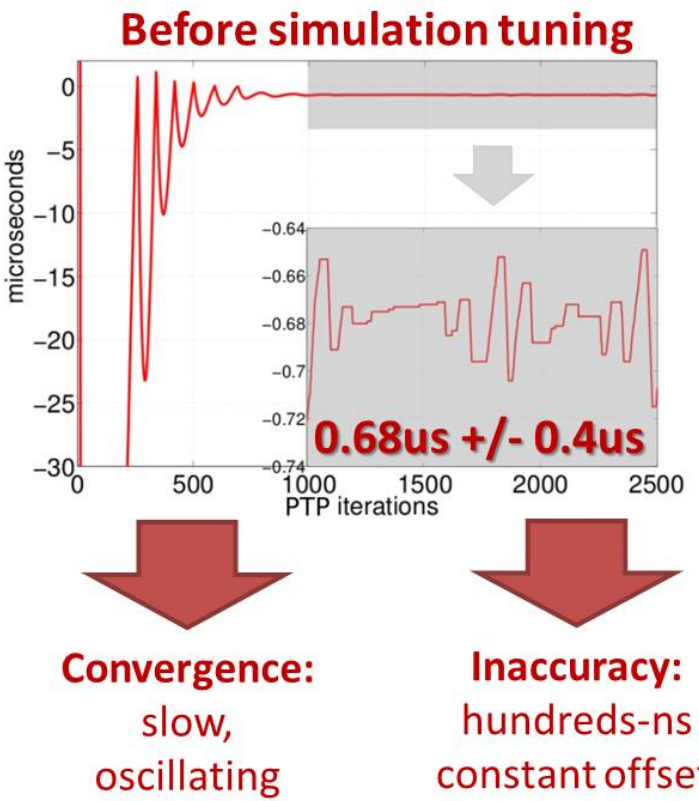

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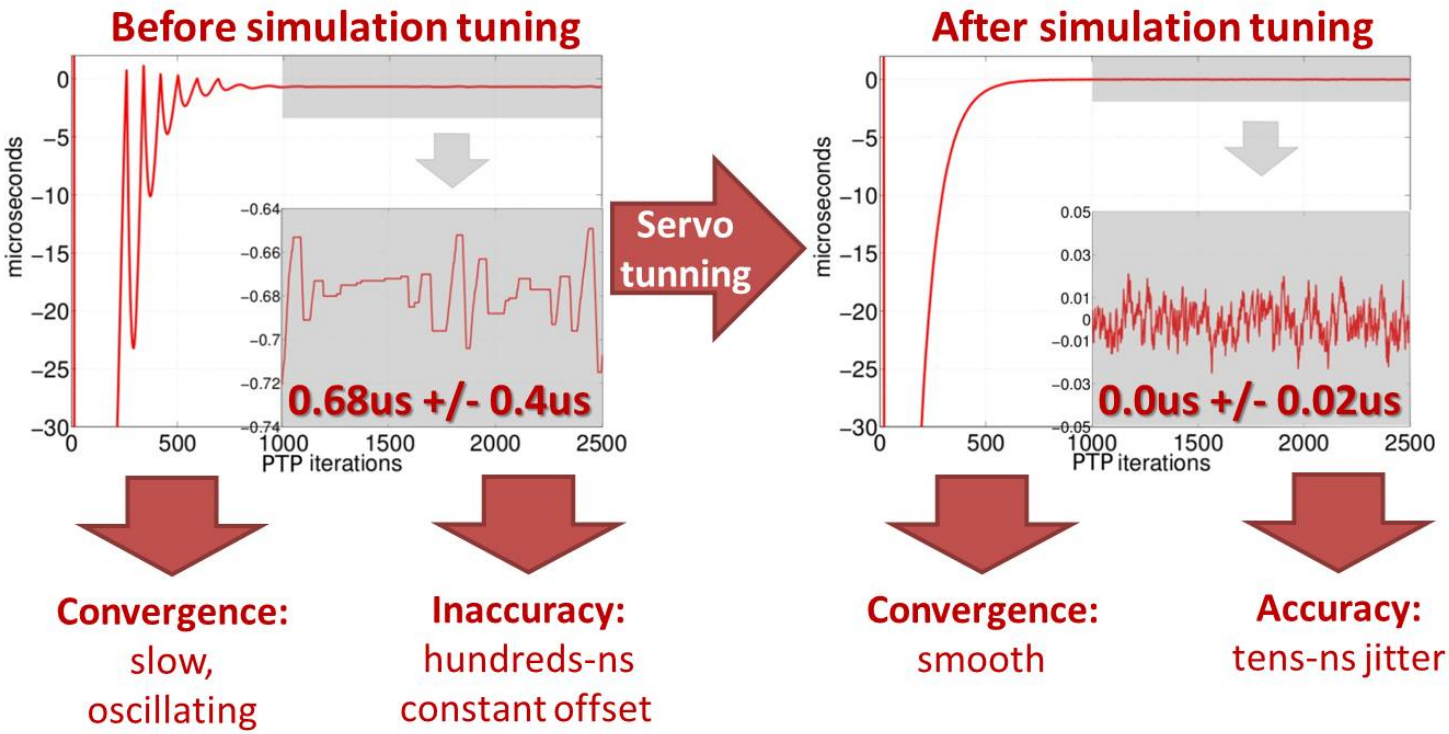

Random fault injection

- Bug report:
  - problem on freestanding node
  - WR PLL not locking when messages lost
- Debugging: random message drop implementation
- PPSi design benefit:
  - available in all architectures
  - useful for non-WR servo simulation-testing

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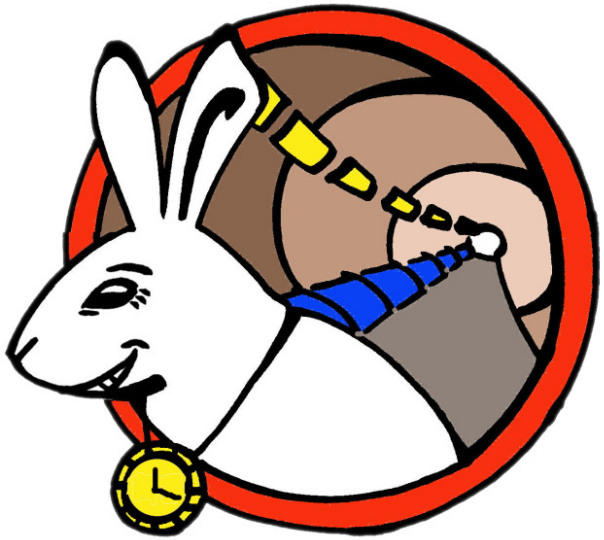
- Layered design
- Abstracted interactions between layers
- Active and ever-growing users community

Questions and answers



Thank you

`www.ohwr.org/projects/ppsi`