Introduction to White Rabbit

Greg Daniluk, Maciej Lipiński

CERN BE-CO
Hardware and Timing section

BE seminar
15 November 2019

Outline

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What is White Rabbit?

- CERN and GSI initiative for control & timing

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- Based on well-established standards
  - Ethernet (IEEE 802.3)
  - Bridged Local Area Network (IEEE 802.1Q)
  - Precision Time Protocol (IEEE 1588)

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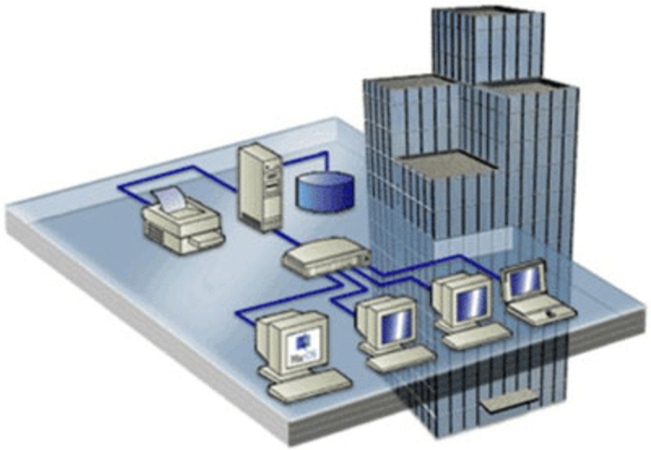

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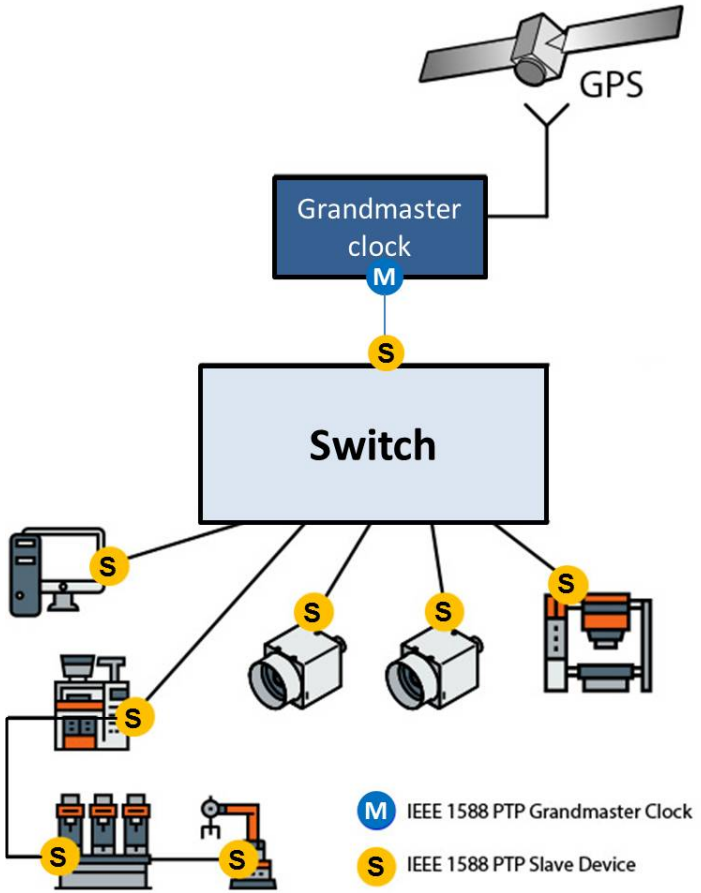

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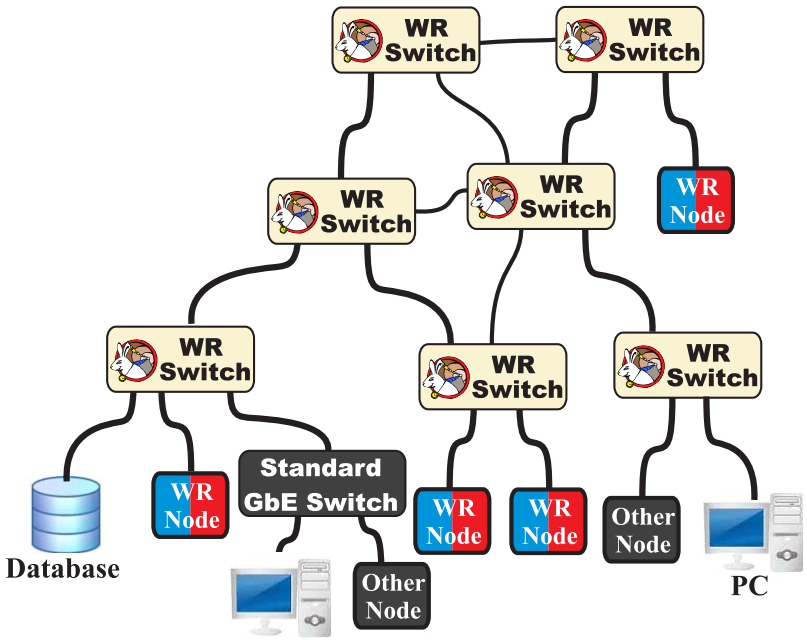
- Extends standards to provide
  - Sub-ns synchronisation
  - Deterministic data transfer



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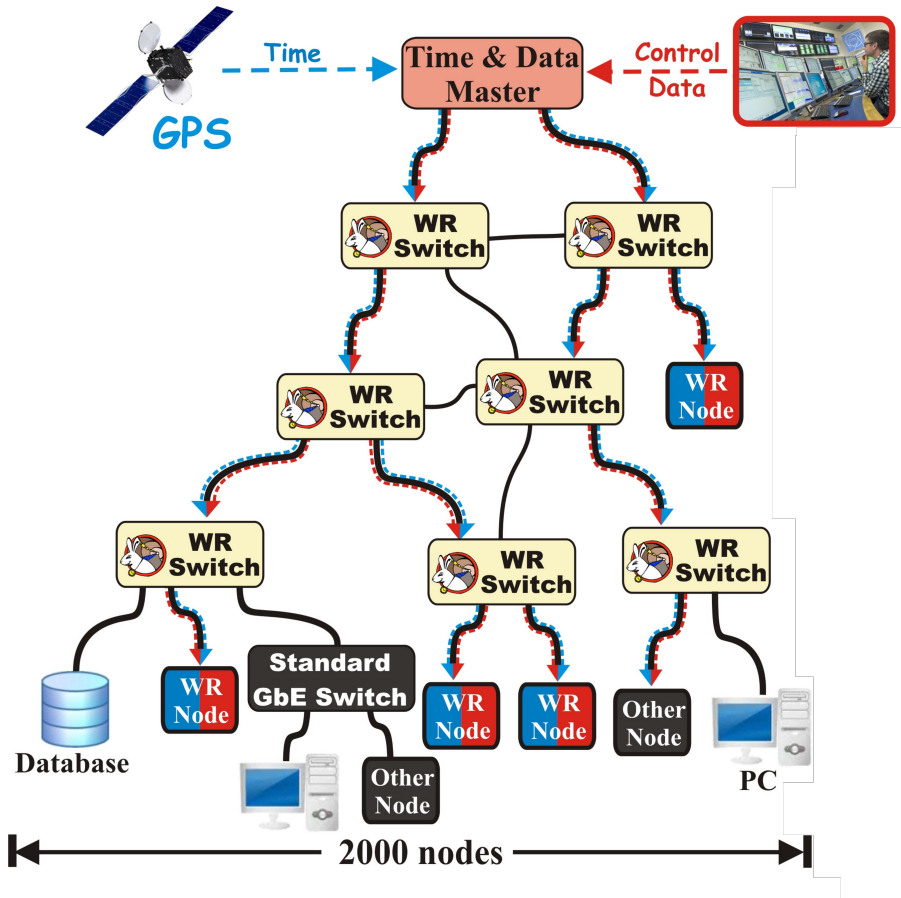

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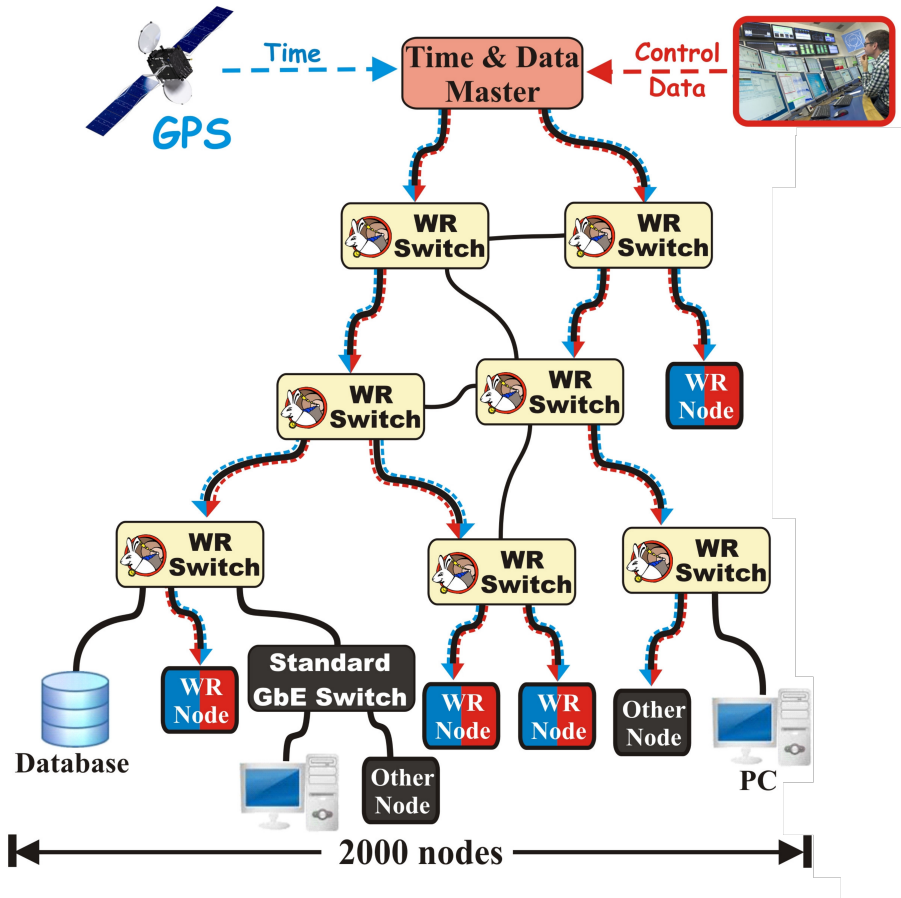

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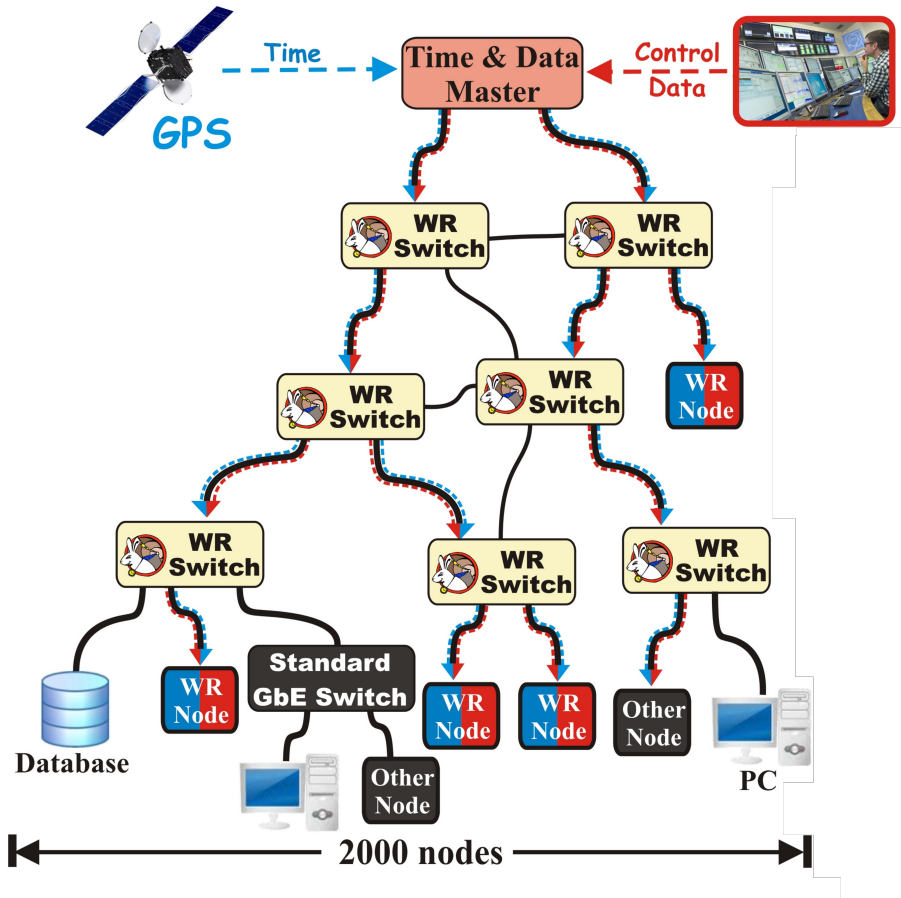
- **Open Source and commercially available**



Many users worldwide, including metrology labs...

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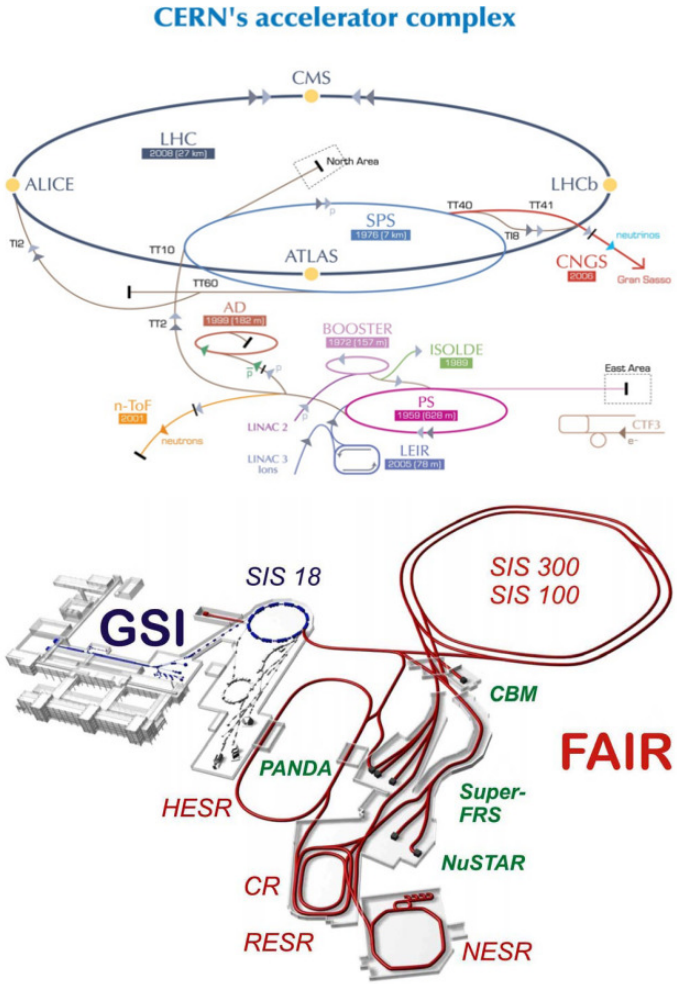

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- CERN and GSI
- The Large High Altitude Air Shower Observatory

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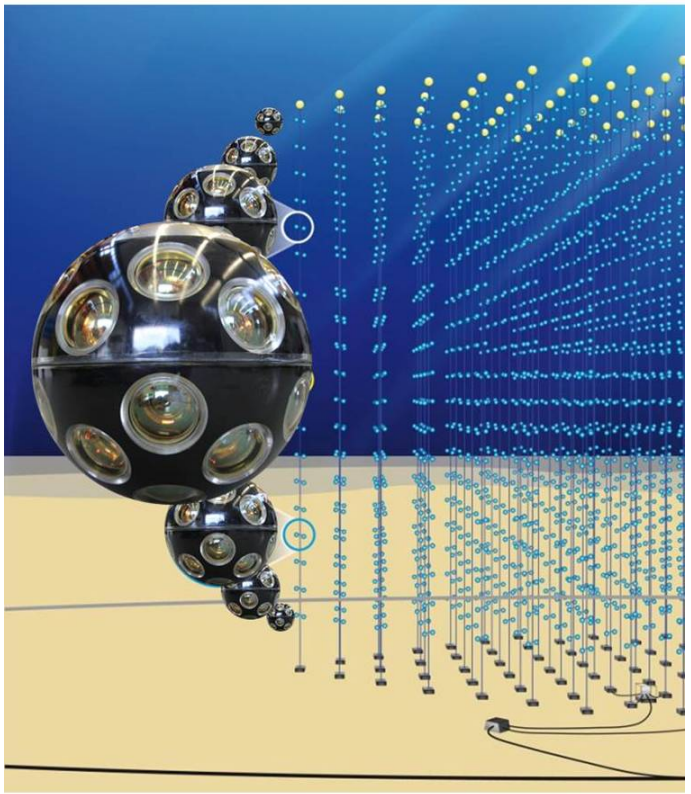
- KM3NET: Cubic Kilometre Neutrino Telescope



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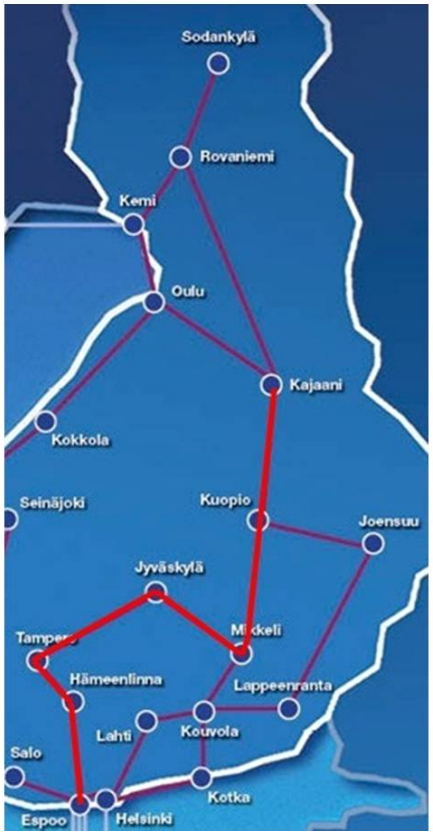
MIKES

The longest WR link of 950 km



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See user page: `http://www.ohwr.org/projects/white-rabbit/wiki/WRUsers`

Outline

White Rabbit technology - sub-ns synchronisation

Based on

- Gigabit Ethernet over fibre
- IEEE 1588 Precision Time Protocol

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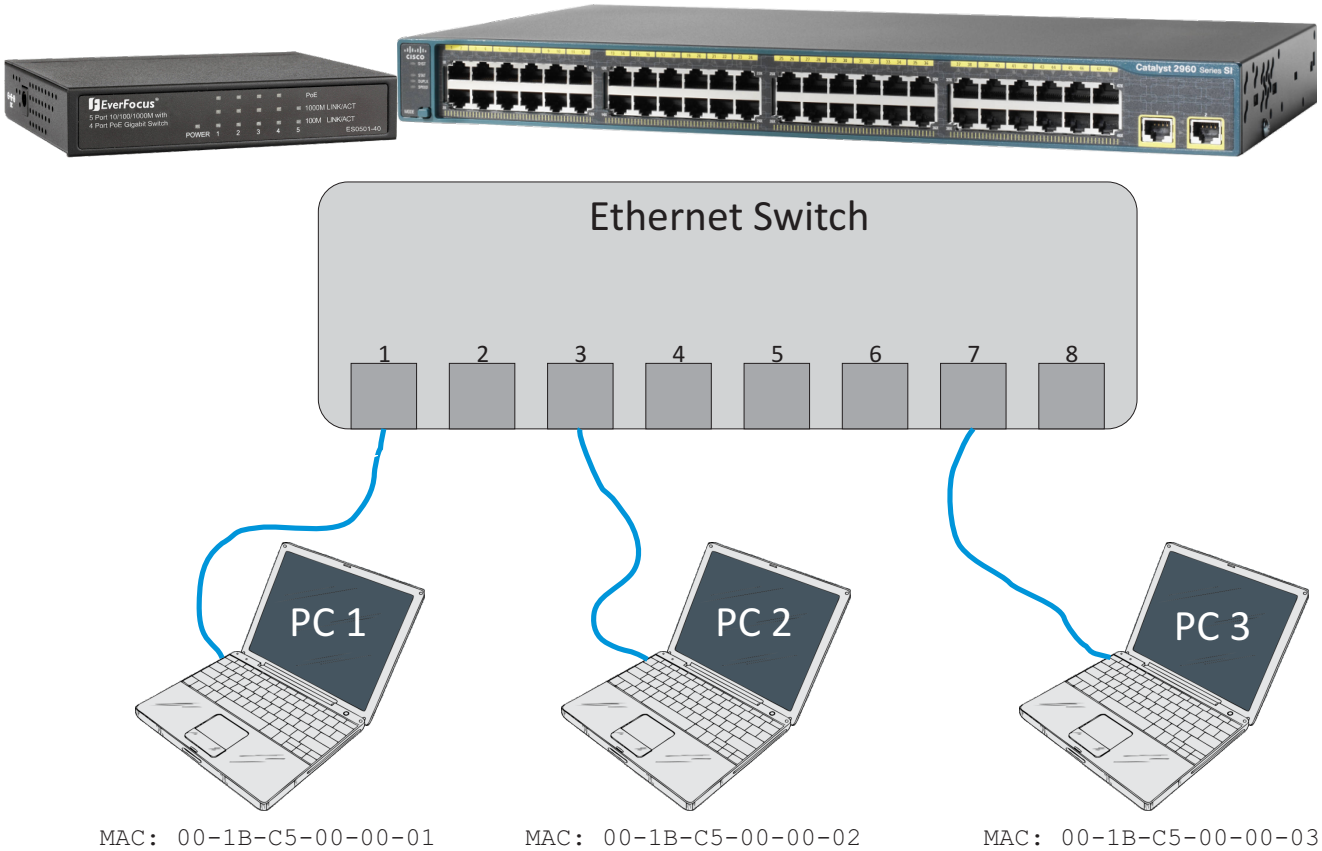
Enhanced with

- Layer 1 syntonisation
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model

Ethernet network in a nutshell



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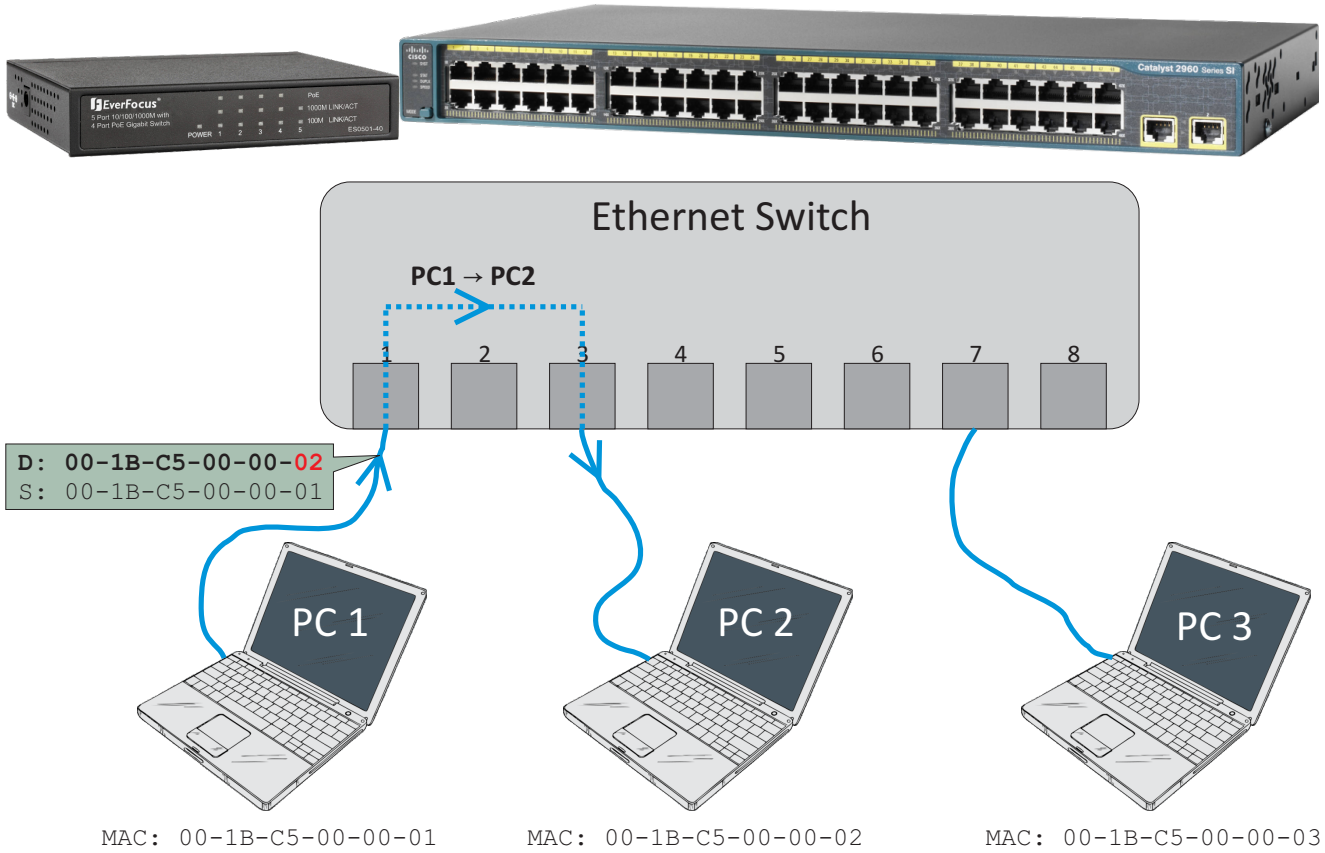

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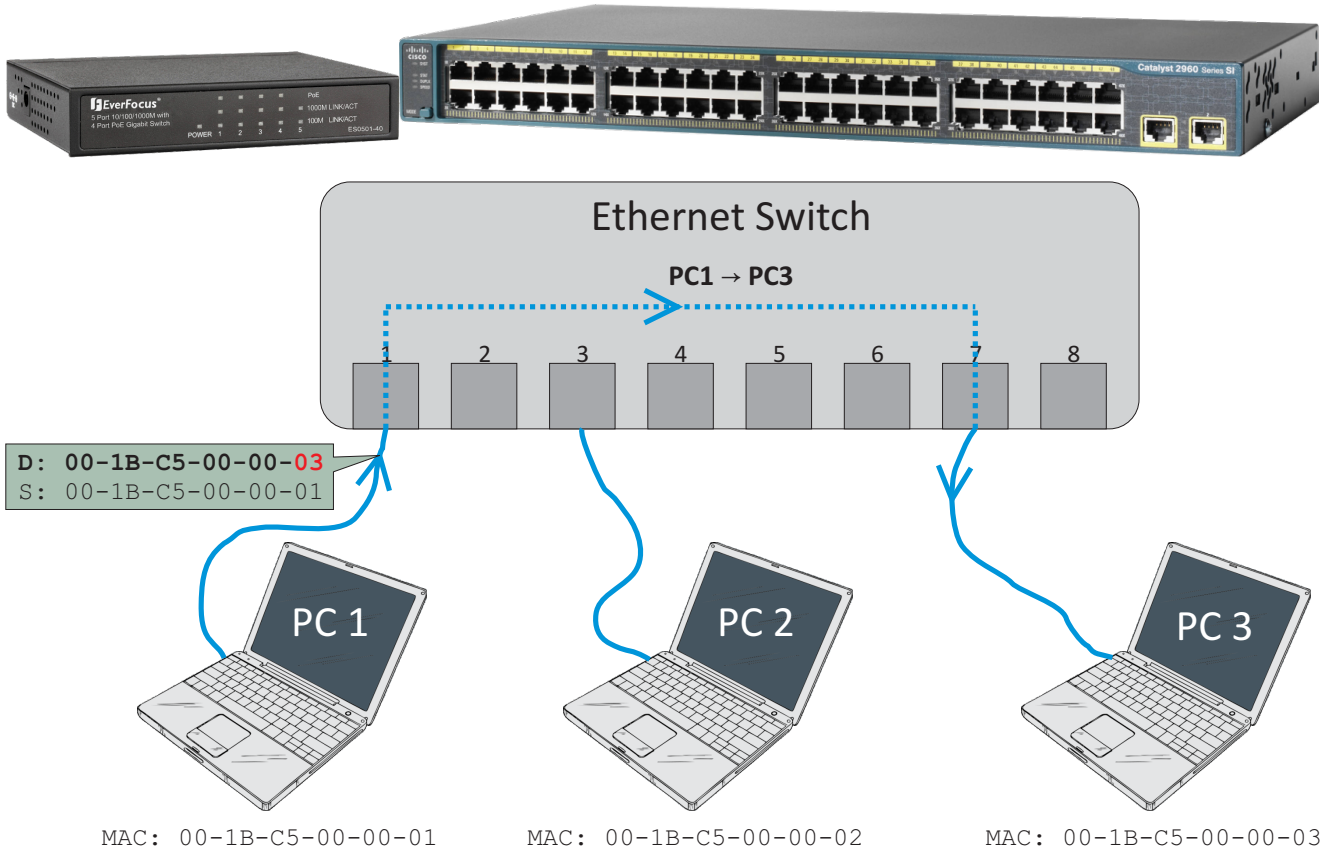

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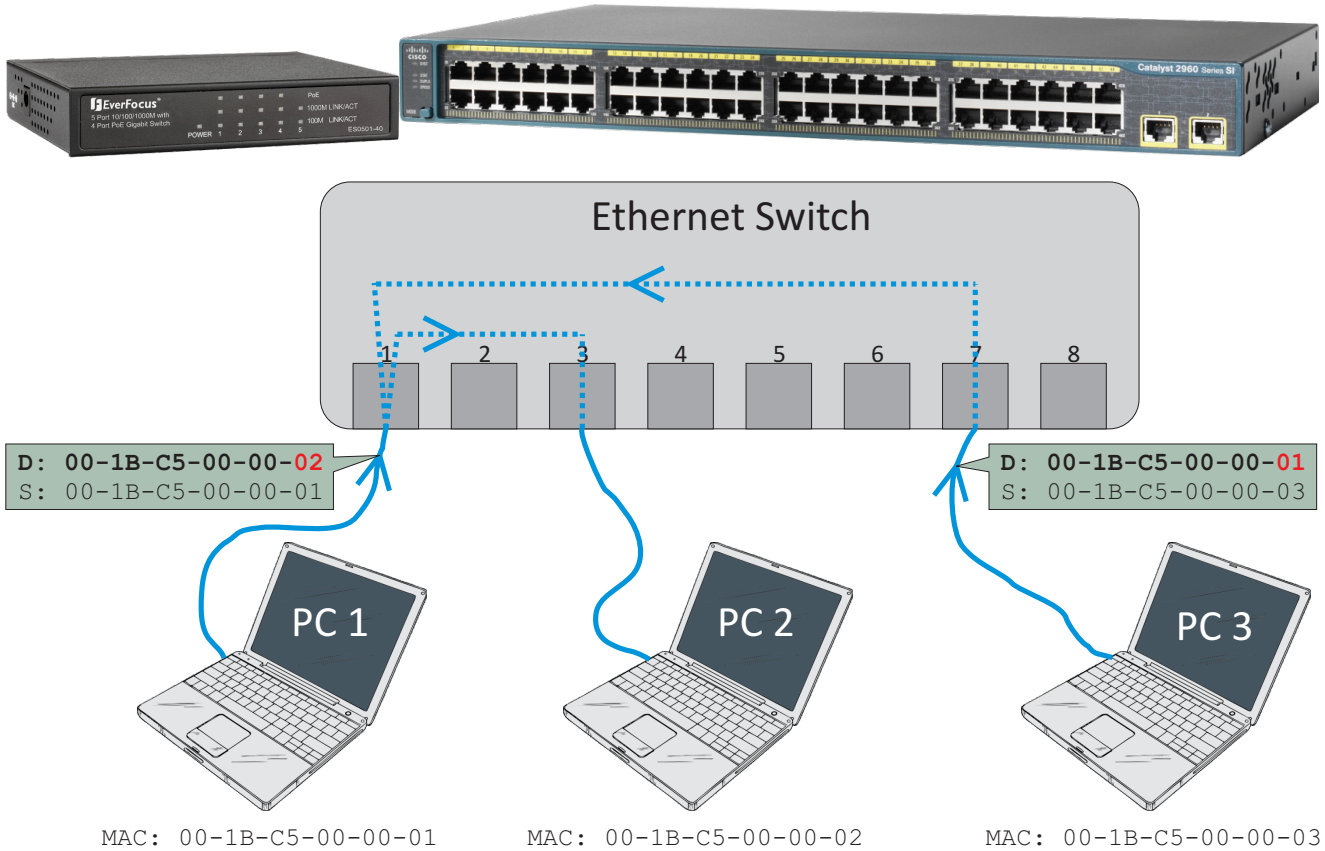
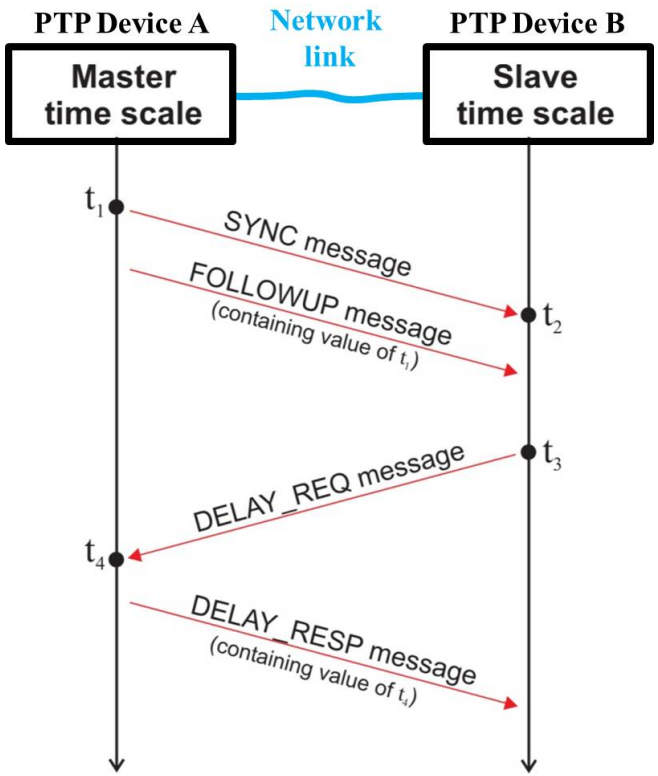


Precision Time Protocol (IEEE 1588)



- Frame-based synchronisation protocol
- Simple calculations:
  - link delay: $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
  - offset from master: $OFM = t_2 - (t_1 + \delta_{ms})$

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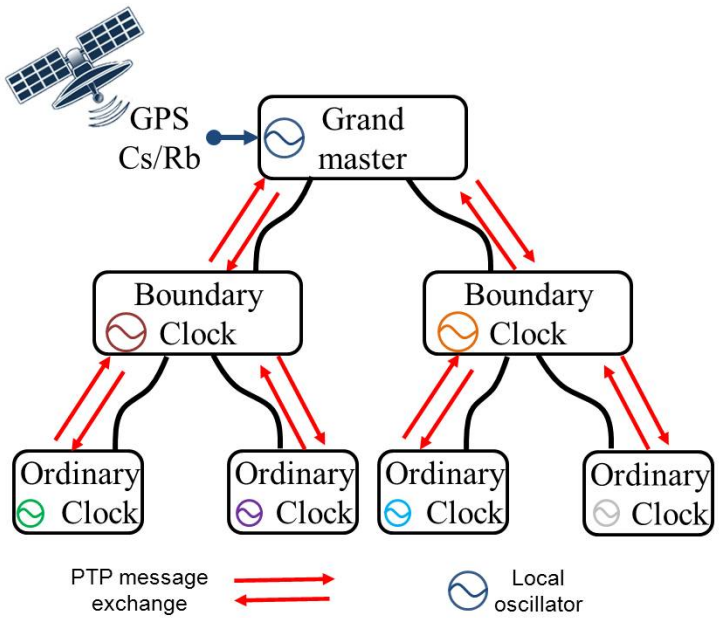

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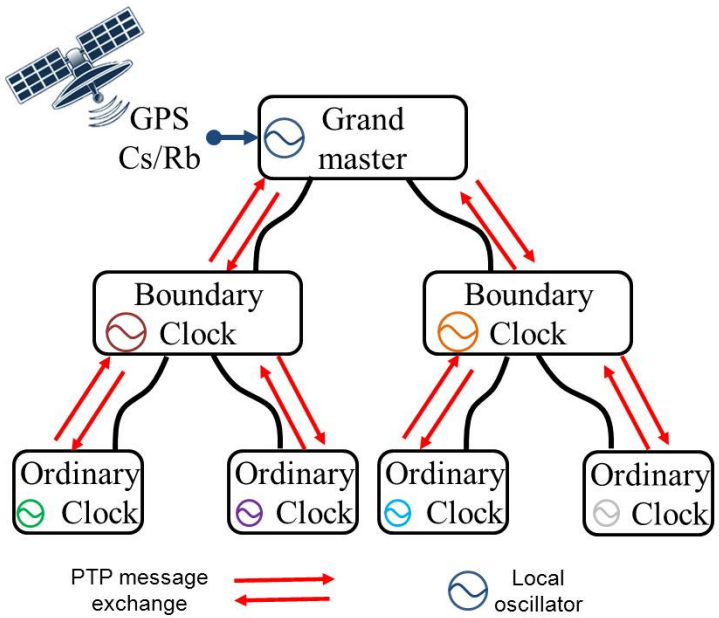

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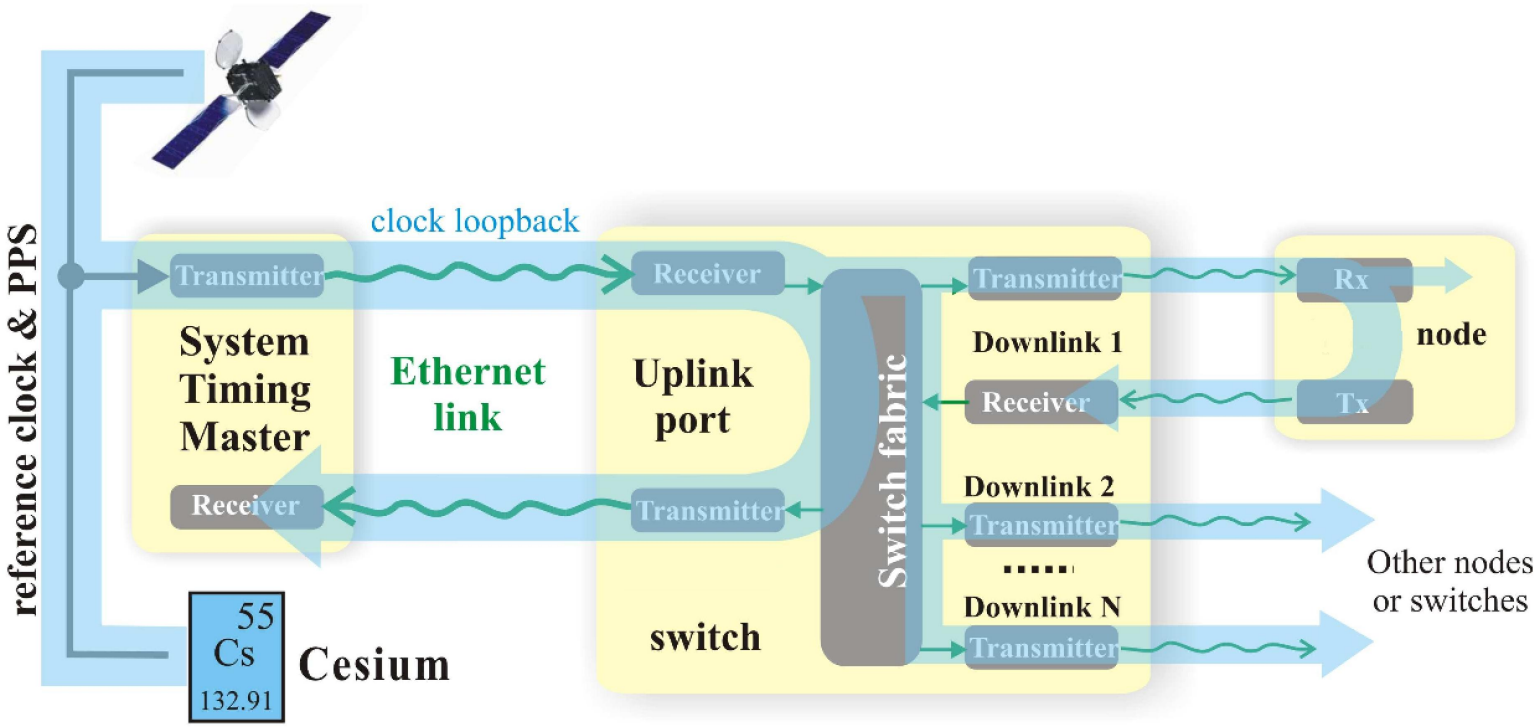
- Shortcomings:
  - devices have free-running oscillators
  - frequency drift compensation vs. message exchange traffic
  - assumes symmetry of medium
  - timestamps resolution

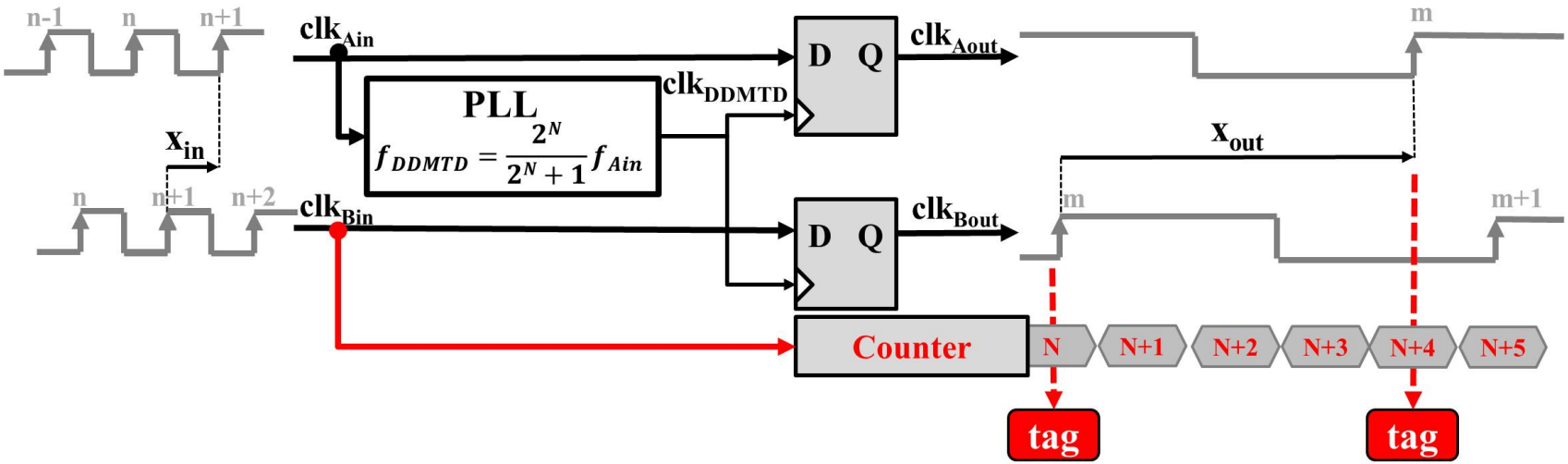
Layer 1 Syntonisation

- Clock is encoded in the Ethernet carrier and recovered by the receiver chip
- All network devices use the same physical layer clock
- Clock loopback allows phase detection to enhance precision of timestamps



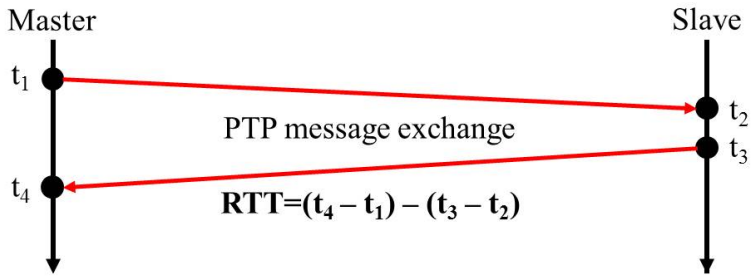
Digital Dual Mixer Time Difference (DDMTD)

- Precise phase measurements in FPGA
- WR parameters:
  - clk_{in} = 62.5 MHz
  - clk_{DDMTD} = 62.496185 MHz (N=14)
  - clk_{out} = 3.814 kHz
- Theoretical resolution of 0.977 ps



Link delay model

- Correction of RTT for asymmetries



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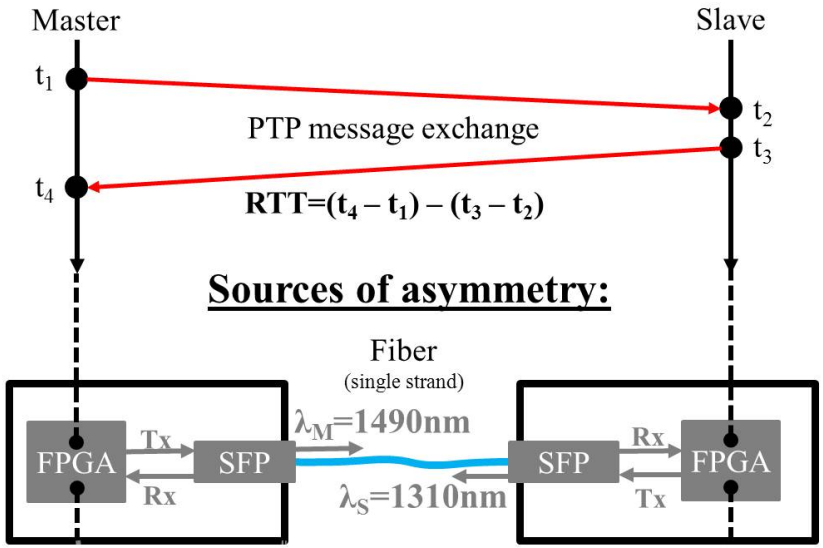

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    $$\alpha = \frac{\nu_g(\lambda_s)}{\nu_g(\lambda_m)} - 1 = \frac{\delta_{ms} - \delta_{sm}}{\delta_{sm}}$$
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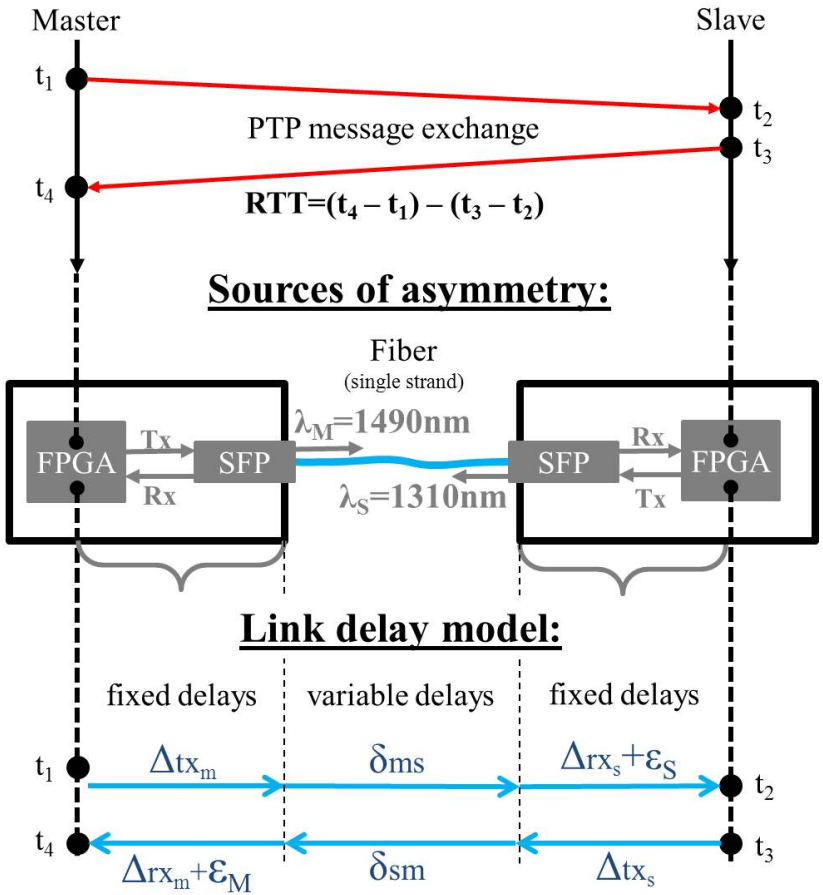

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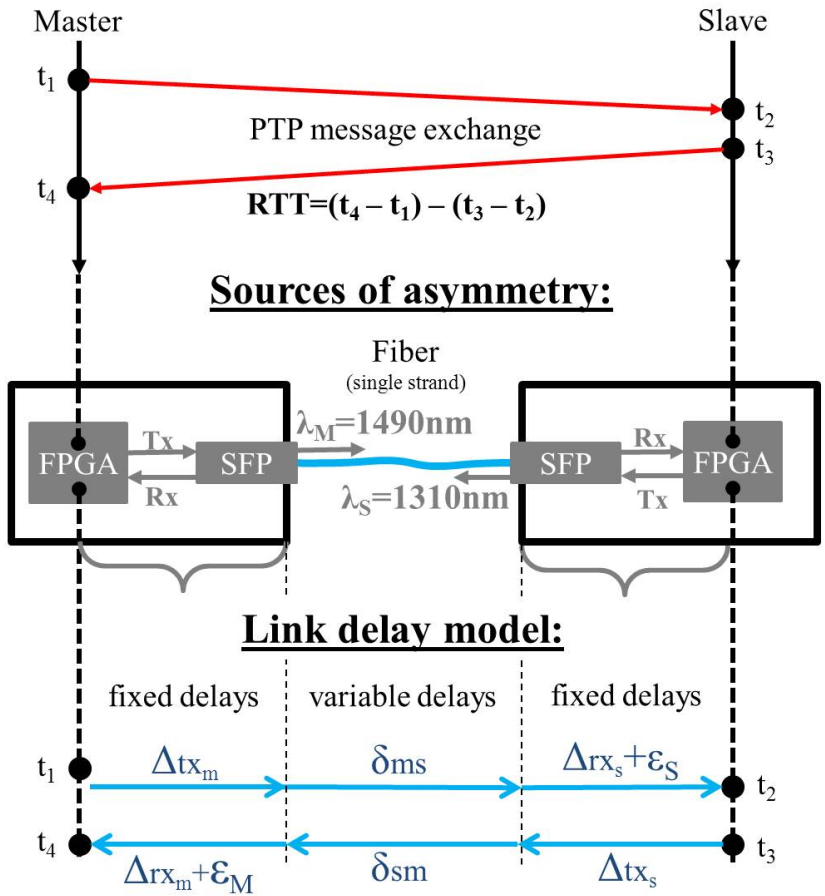
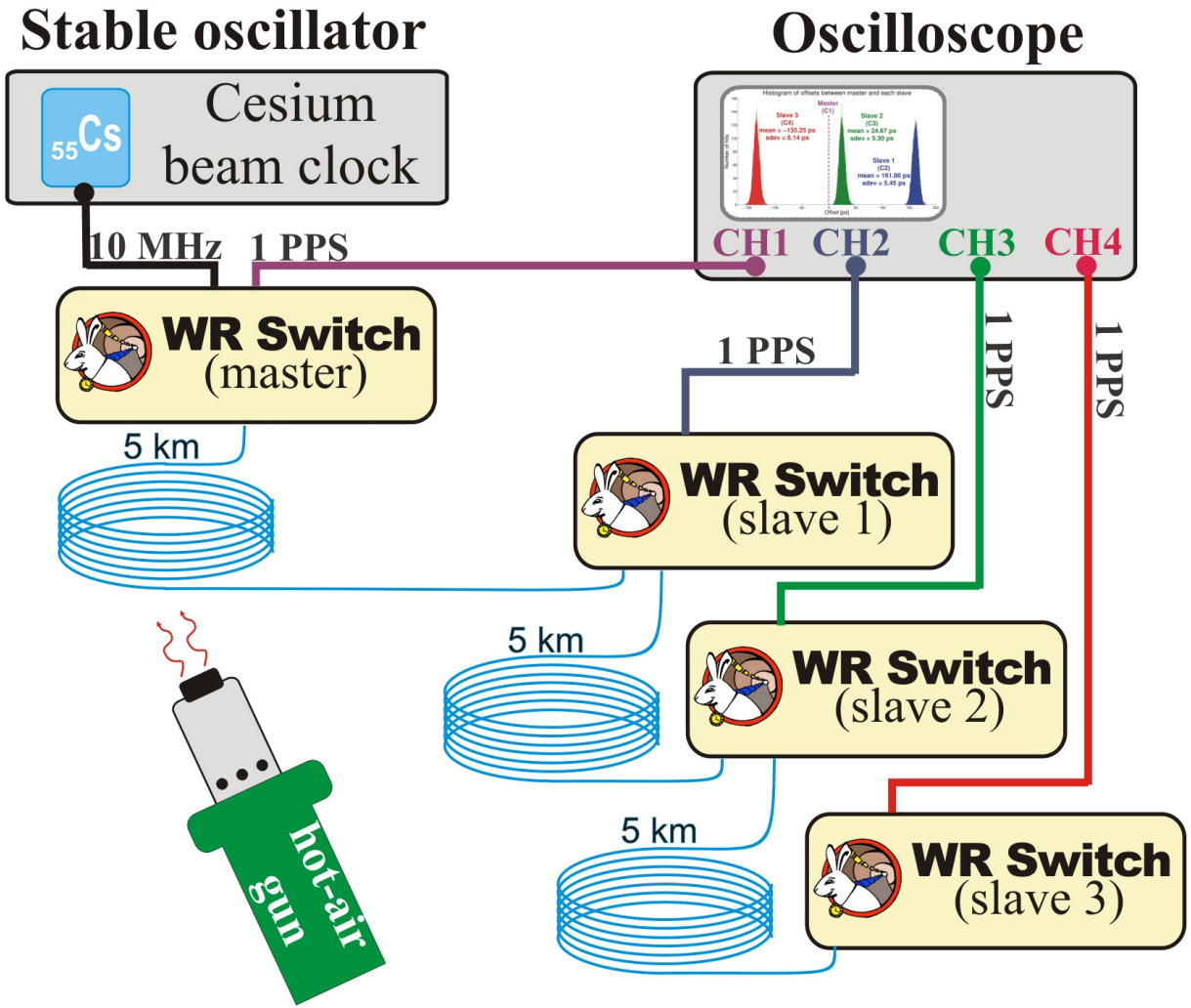
  - Calibration procedure to find fixed delays and α
- Accurate offset from master (OFM):

$$\delta_{ms} = \frac{1+\alpha}{2+\alpha}\left(RTT - \sum \Delta - \sum \epsilon\right)$$

$$OFM = t_2 - (t_1 + \delta_{ms} + \Delta_{txm} + \Delta_{rxs} + \epsilon_S)$$



Out-of-the-box performance



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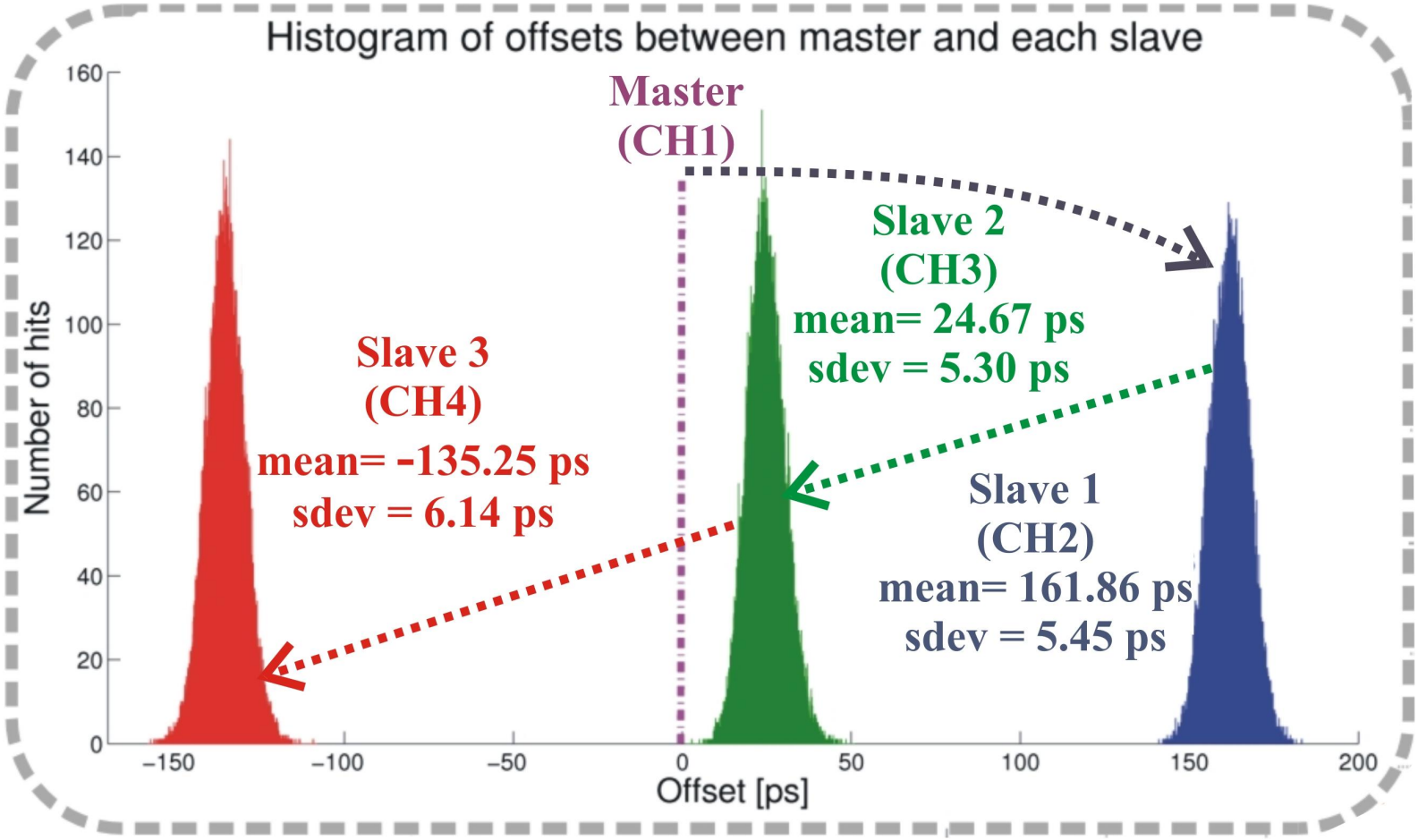
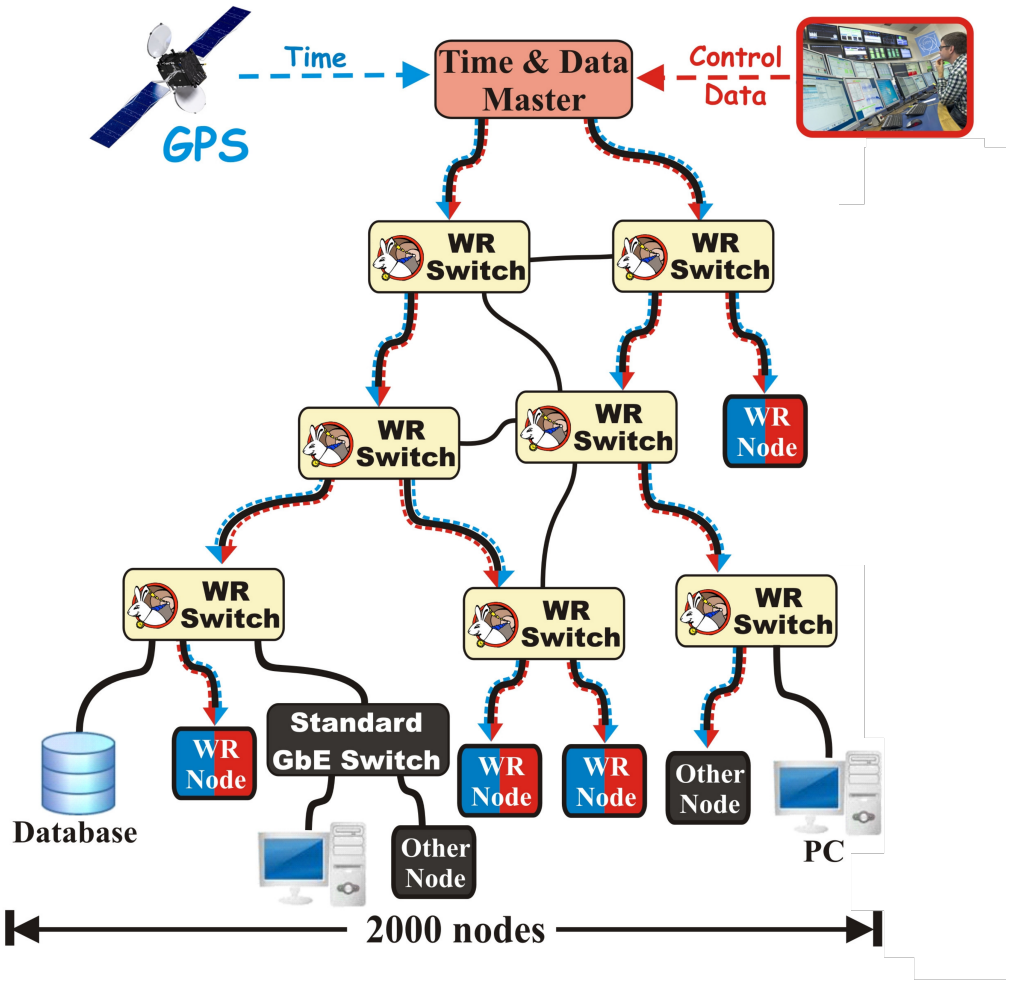


Outline

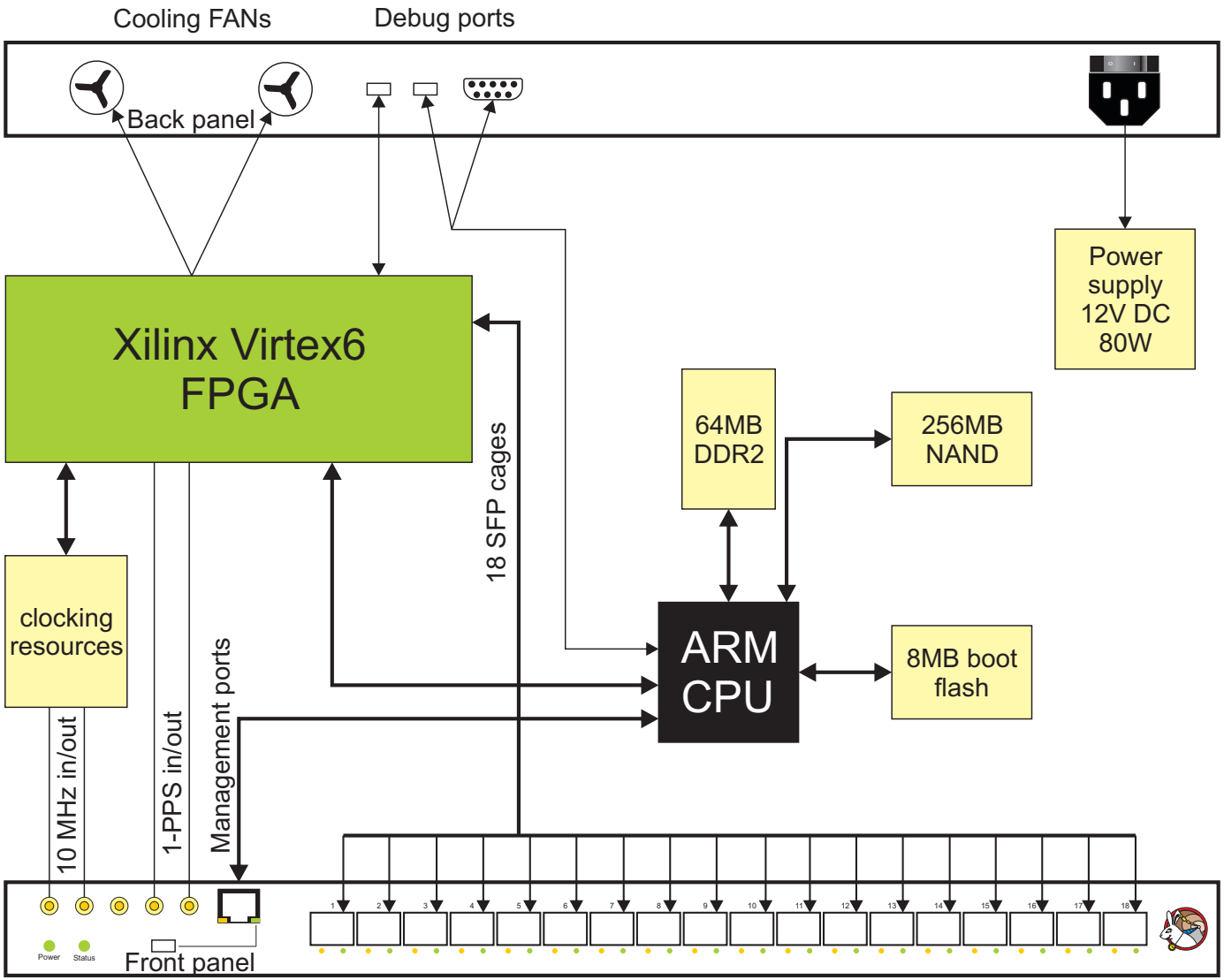
Typical WR network



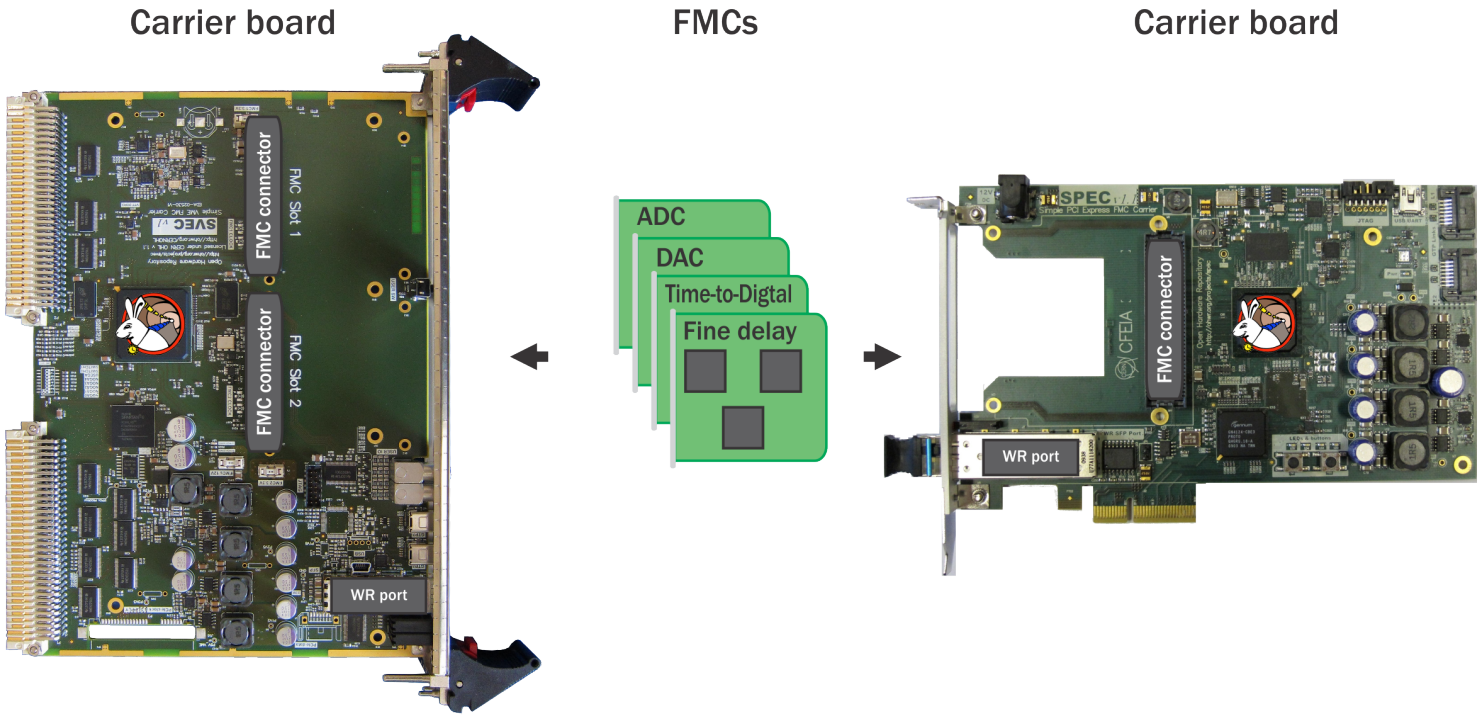
WR Switch

- Central element of WR network
- 18 port gigabit Ethernet switch with WR features
- Default optical transceivers: up to 10km, single-mode fiber
- Fully open, commercially available from 4 companies

WR Switch: hardware block diagram

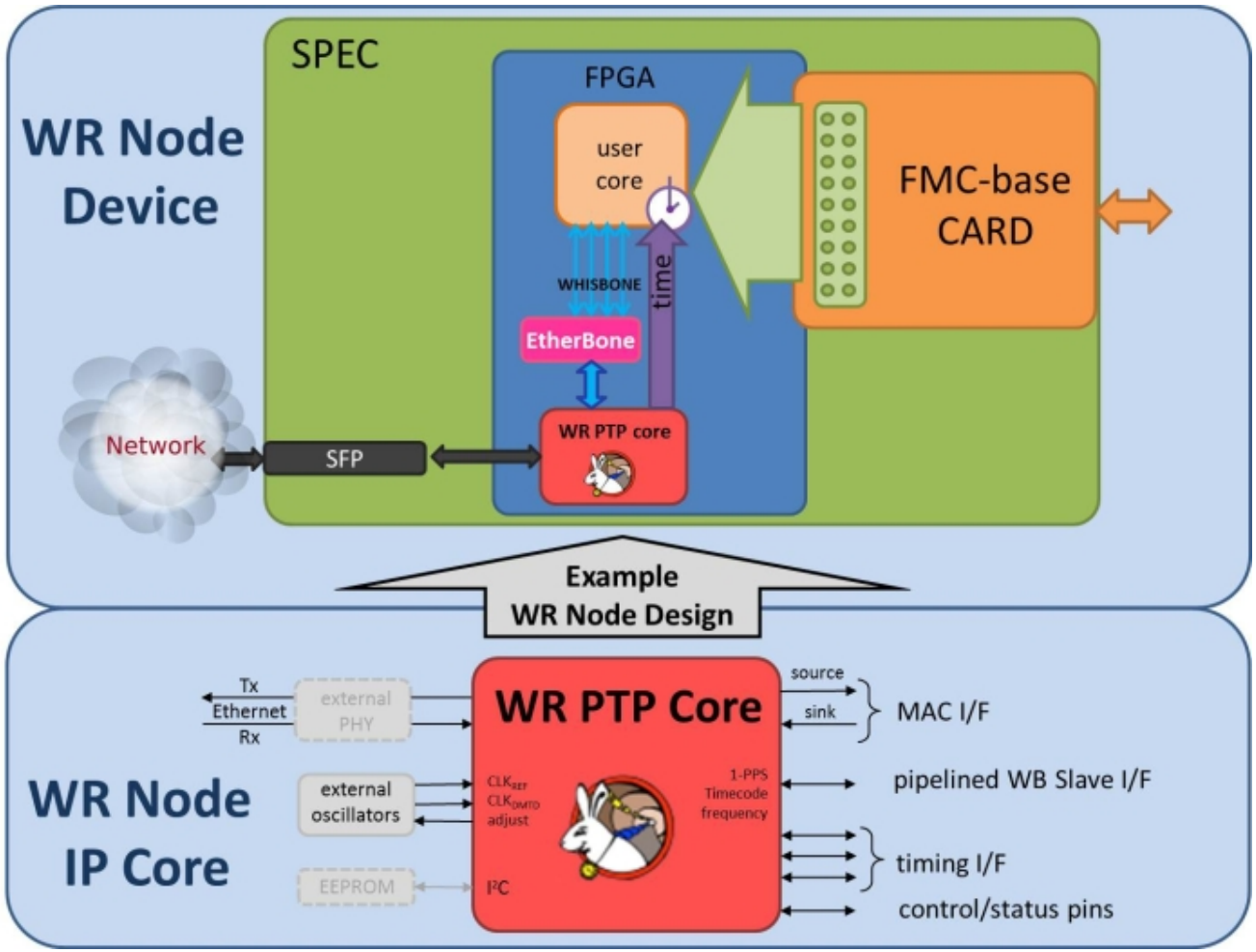


WR Node: carriers + mezzanines



- All carrier cards are equipped with a White Rabbit port
- All carrier cards instantiate WR PTP Core
- Mezzanines can use the accurate clock signal and timecode (synchronous sampling clock, trigger time tag, ...)

WR PTP Core


WR Node Device
SPEC
FPGA
user core
WHISBONE
time
EtherBone
WR PTP core
FMC-base CARD
Network
SFP
Example WR Node Design
WR Node IP Core
Tx
Ethernet
Rx
external PHY
external oscillators
EEPROM
I²C
WR PTP Core
source
sink
MAC I/F
1-PPS
Timecode
frequency
pipelined WB Slave I/F
timing I/F
control/status pins

Open **and** commercially available off-the-shelf

WR Switch

Seven Sol, Spain
Creotech, Poland

OPNT, Netherlands
SyncTechnology, China

Simple VME FMC carrier (SVEC)
Janz Tec AG, Germany

Simple PCIe FMC carrier (SPEC)
Creotech, Poland
INCAA, Netherlands
Seven Solutions, Spain
ISD S.A., Greece

Compact Universal Timing Endpoint (Cute-WR-DP)
SyncTech, China

Digitizers
Struck, Germany
SP Devices, Sweden

GPS Disciplined Oscillator
Seven Solutions, Spain

ZEN TP-32 BNC
Seven Solutions, Spain

PXI module
Sundance, UK

Companies selling White Rabbit:

`www.ohwr.org/projects/white-rabbit/wiki/wrcompanies`

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Management of WR networks: monitoring & config

- White Rabbit is an extension of Ethernet

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- It can be managed using standard protocols and tools:
  - Simple Network Management Protocol (SNMP)
  - Syslog
  - Link Layer Discovery Protocol (LLDP)
  - Kerberos-based authentication

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- It can be managed using standard protocols and tools:
  - Simple Network Management Protocol (SNMP)
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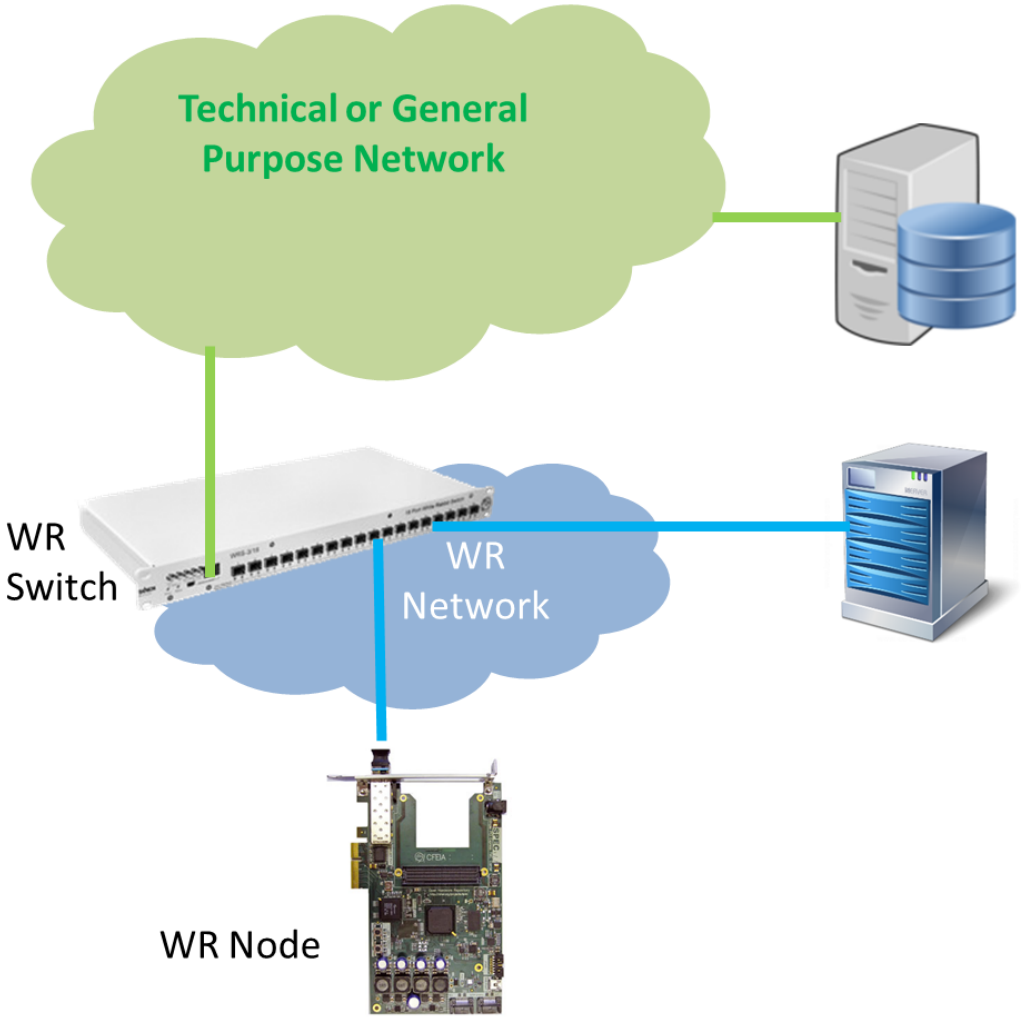
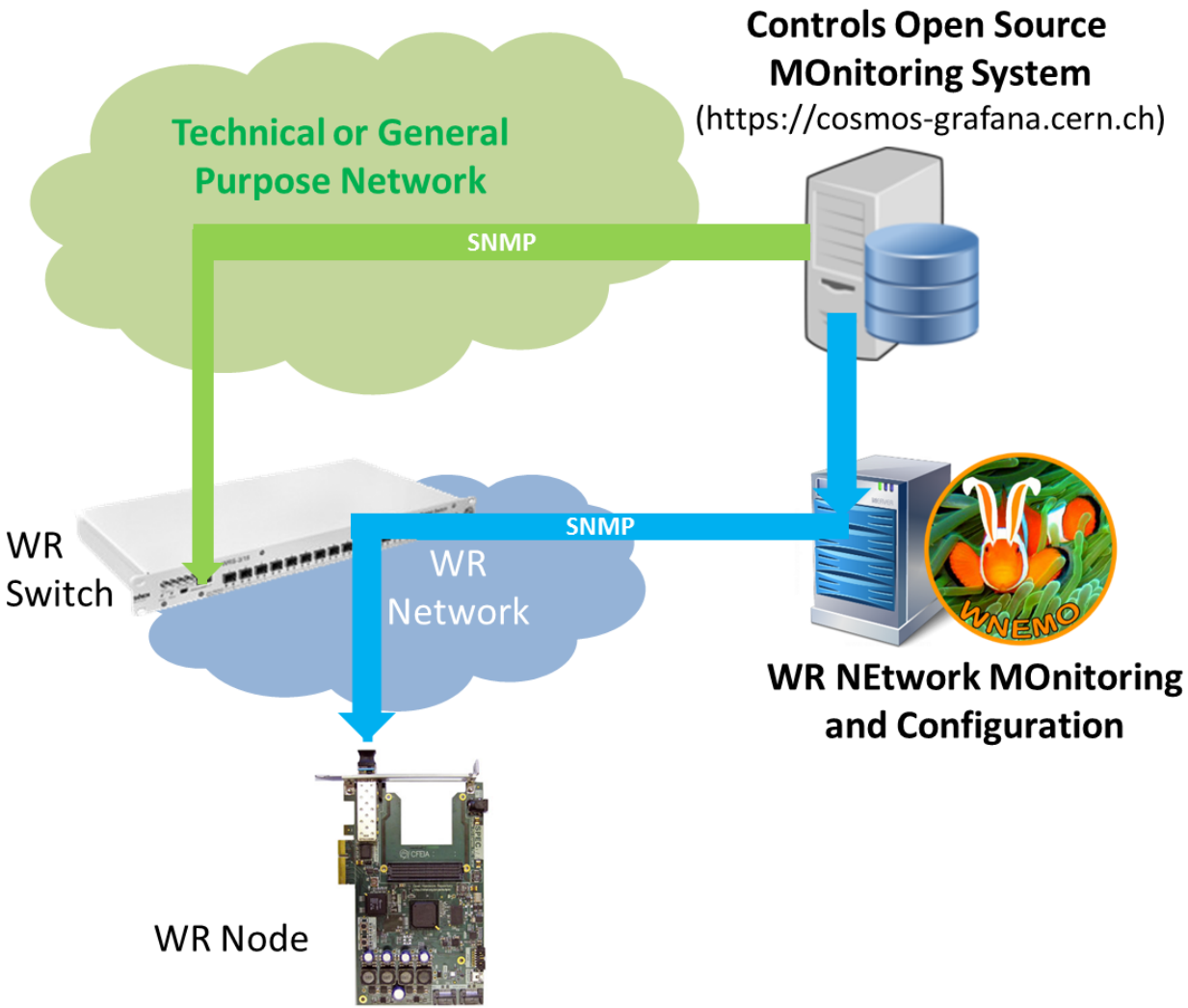
- It can be debugged using standard tools:
  - Wireshark
  - Tcpdump
  - Professional Ethernet testers

WR Network vs. TN/GPN Network



BE-CO services: Monitoring with COSMOS/Grafana



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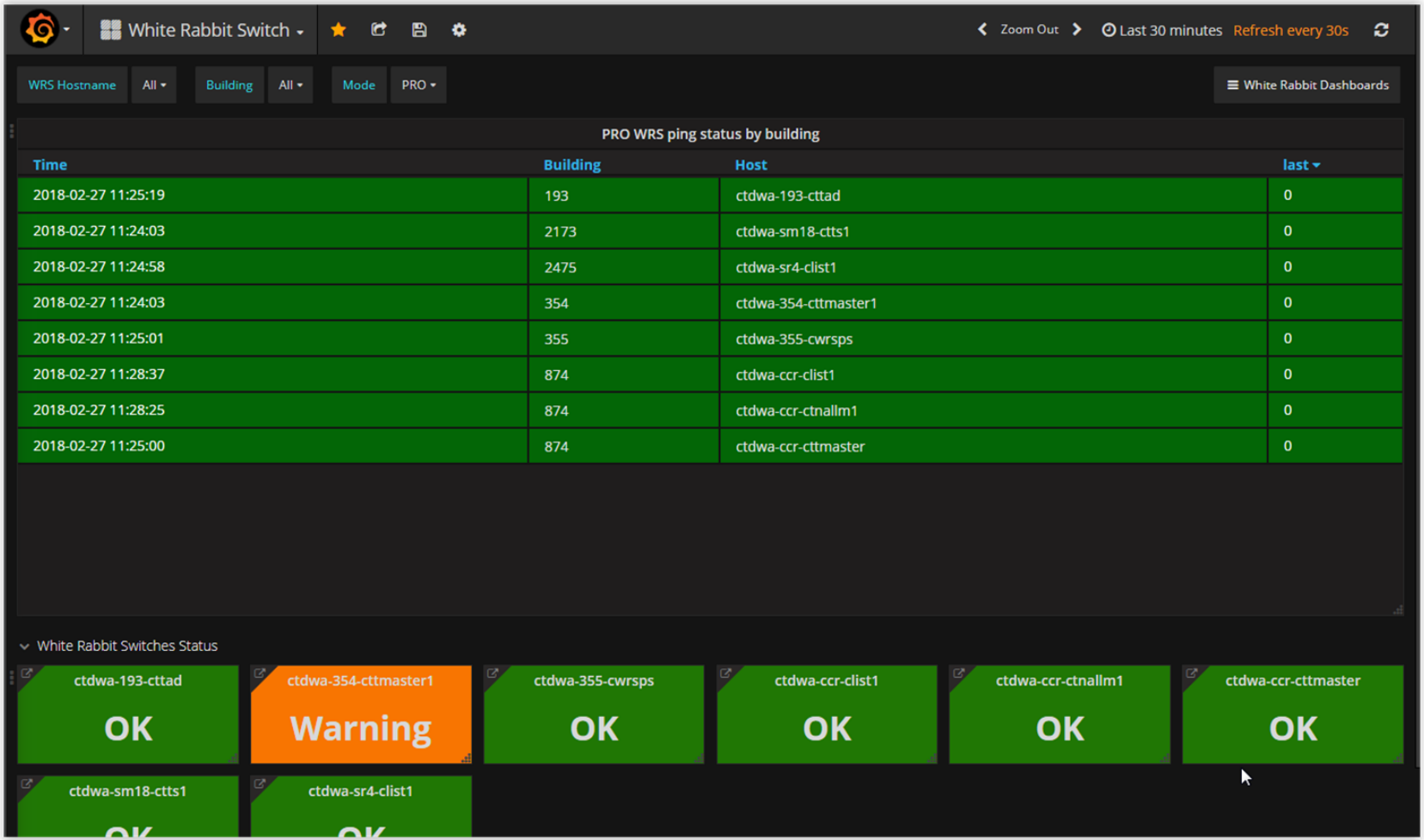
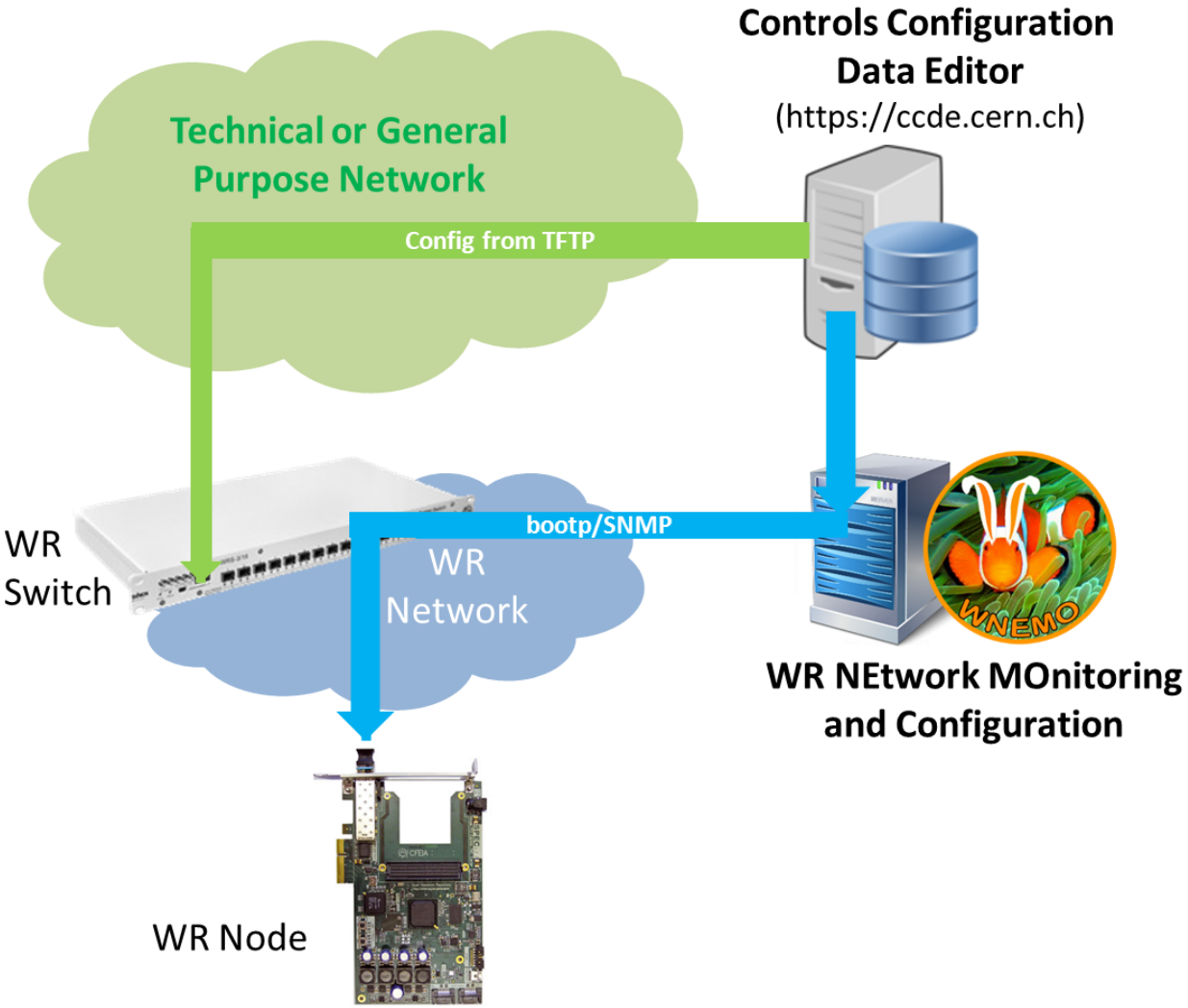


BE-CO services: Configuration with CCDE



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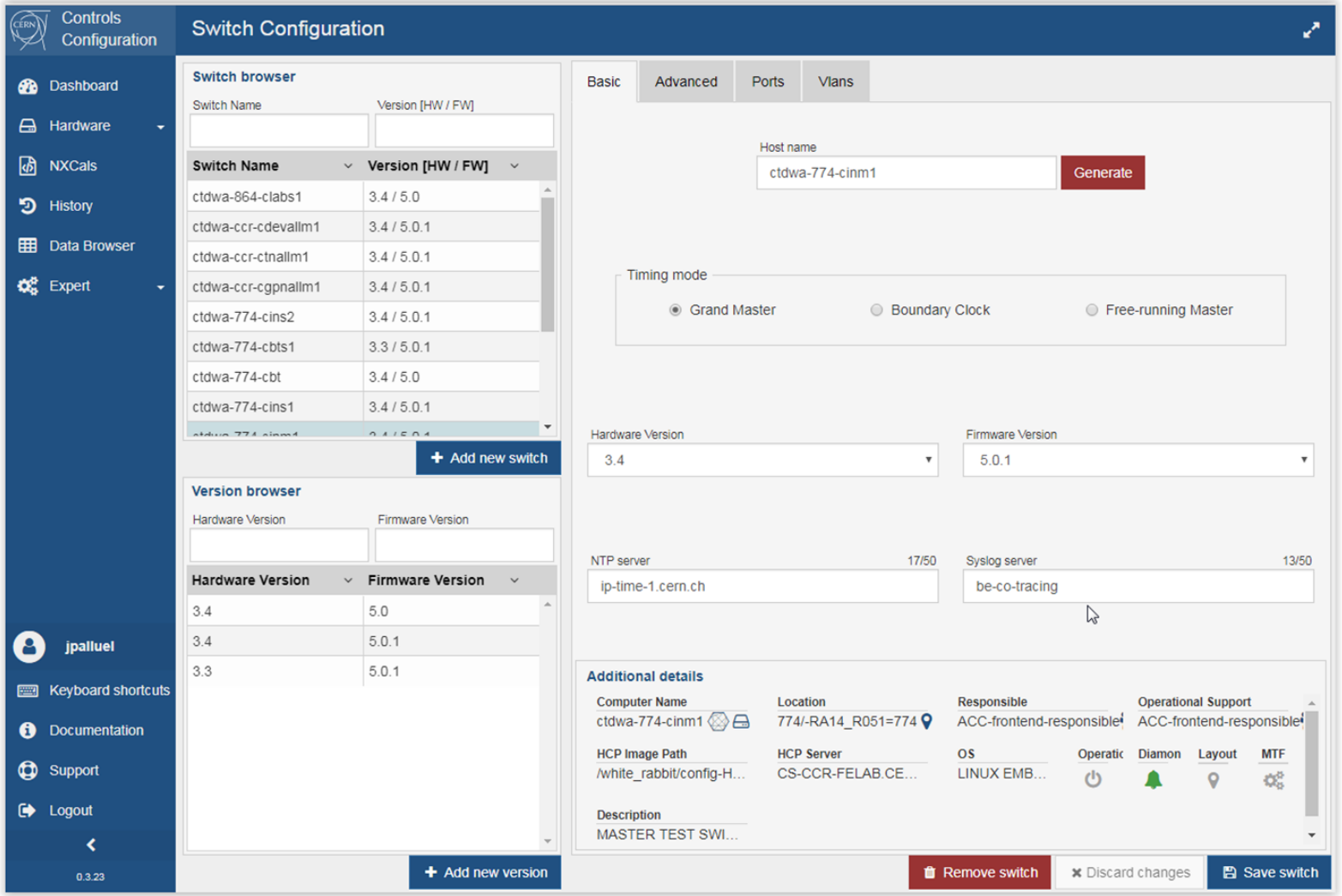

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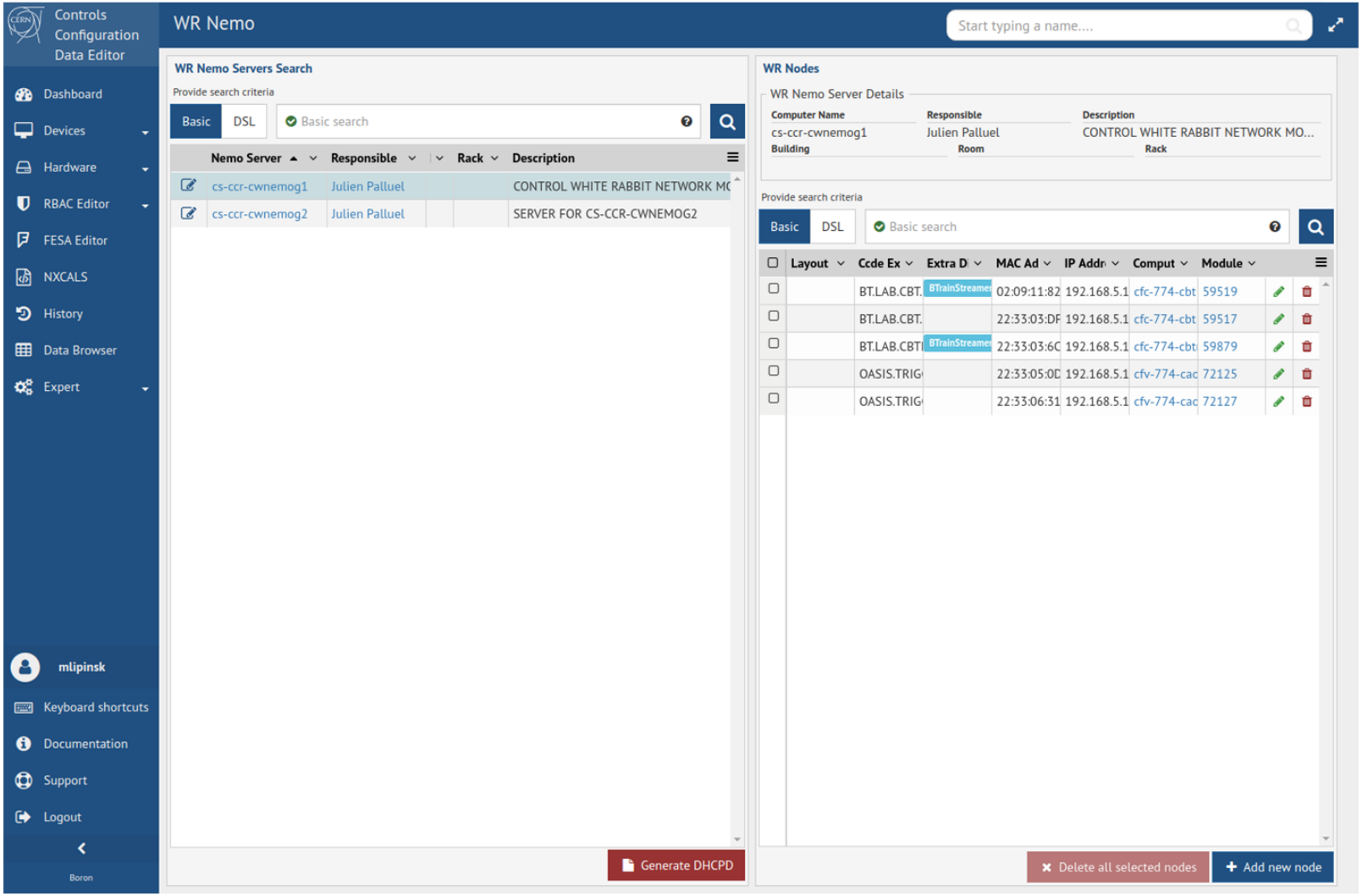

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WR applications in science and beyond

- Time & frequency transfer
- Time-based control
- Precise timestamping
- Trigger distribution
- Fixed-latency data transfer
- Radio-frequency transfer

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NOTE

Selected
WR applications at CERN
will be detailed
next week

Time & frequency transfer

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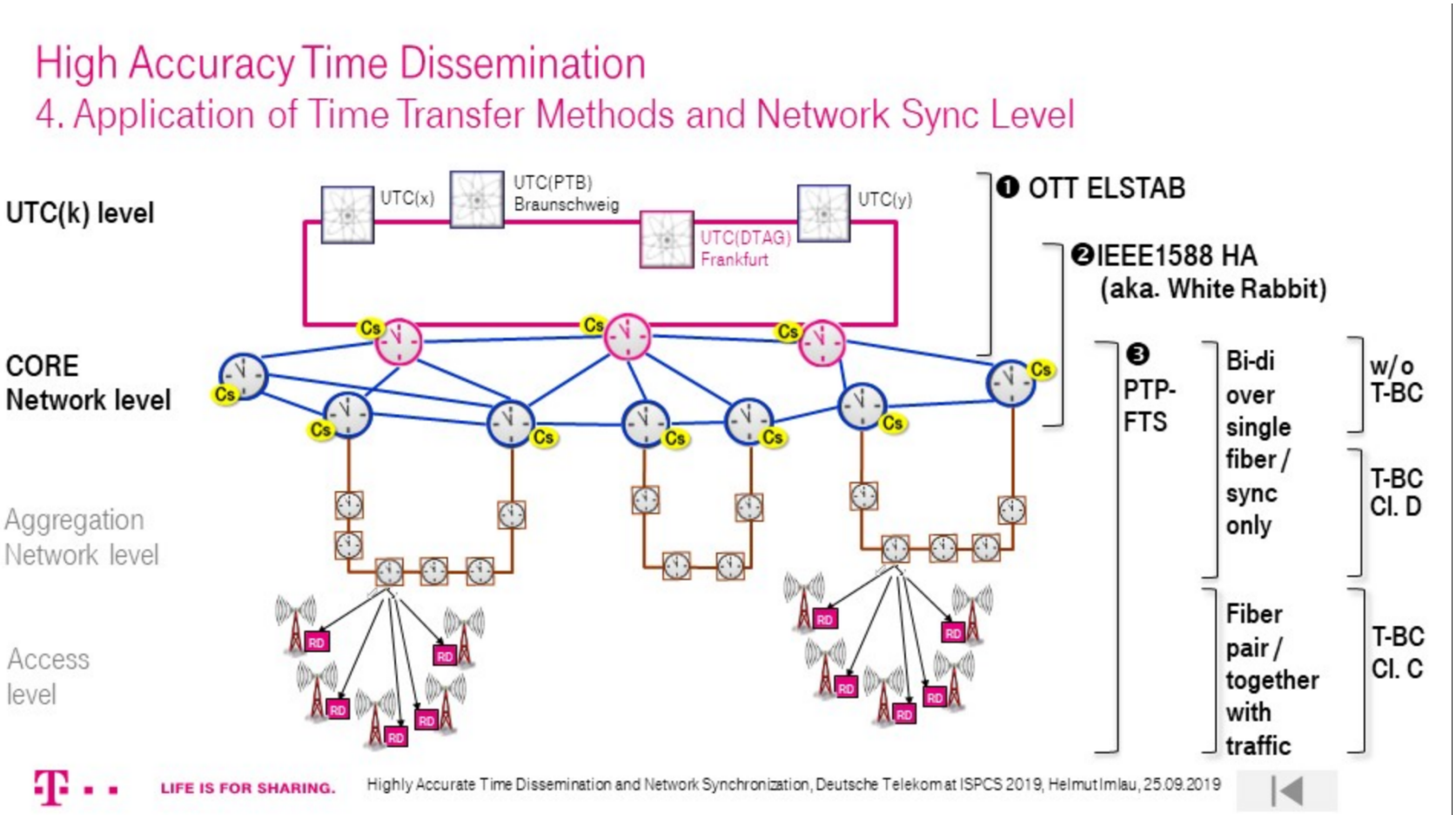
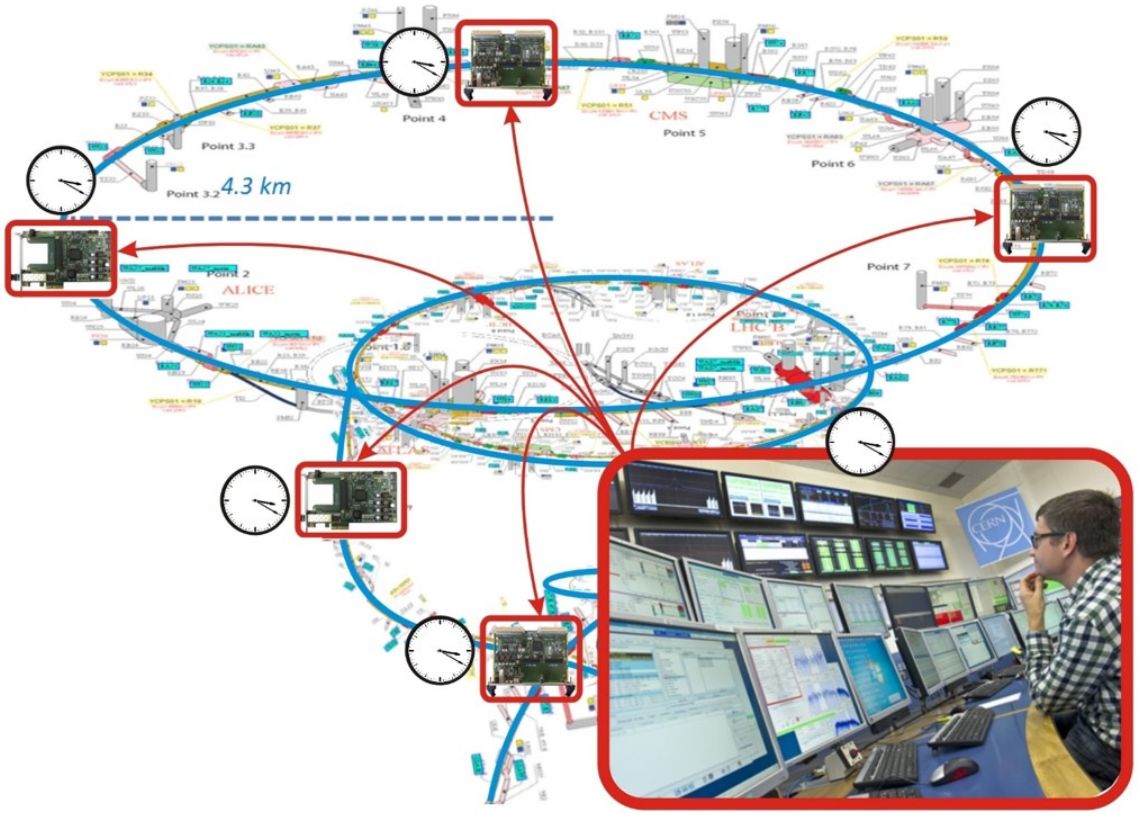
- Evaluated by Deutsche Telecom



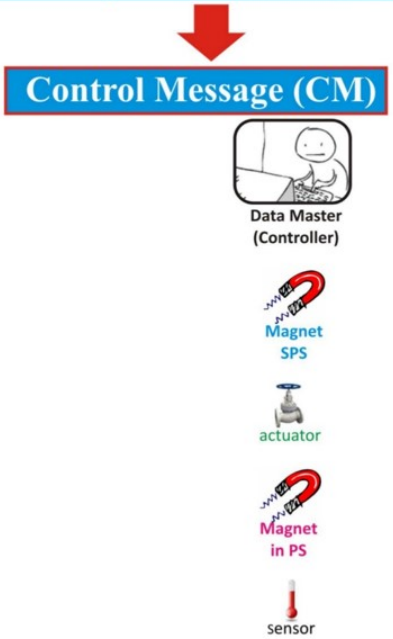
ISPCS keynote *Highly Accurate Time Dissemination & Network Synchronisation*, Helmut Imlau, Deutsche Telekom

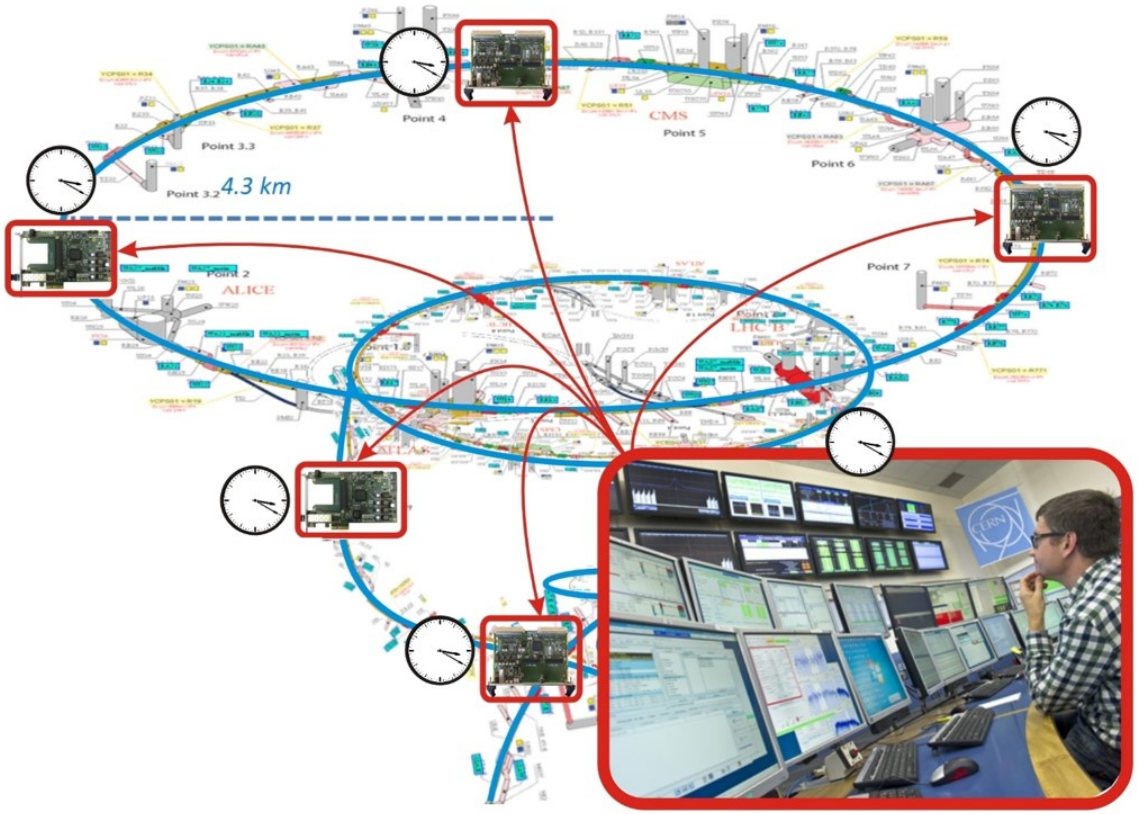
Time-based control



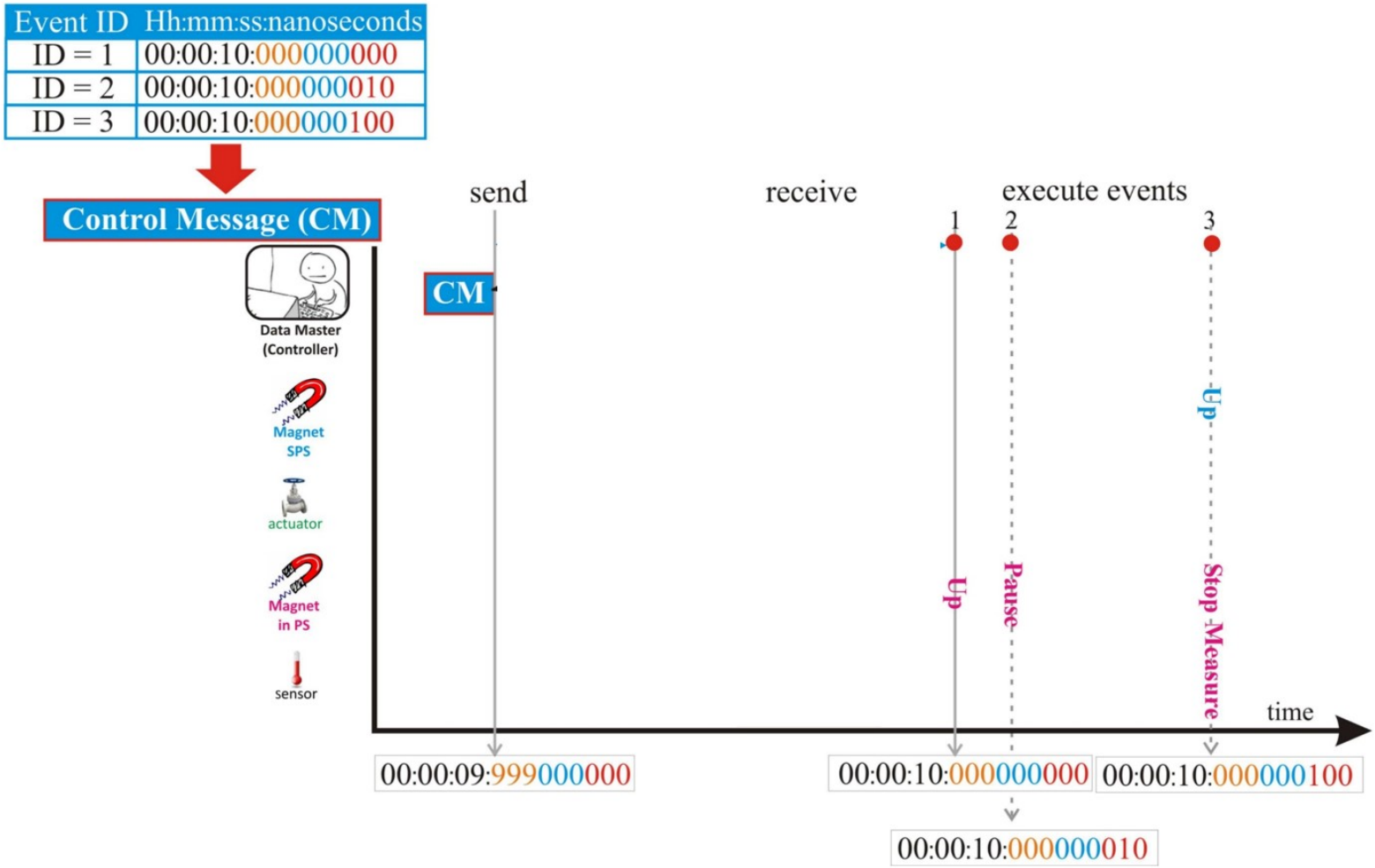
Time-based control

Event ID	Hh:mm:ss:nanoseconds
ID = 1	00:00:10:000000000
ID = 2	00:00:10:000000010
ID = 3	00:00:10:000000100



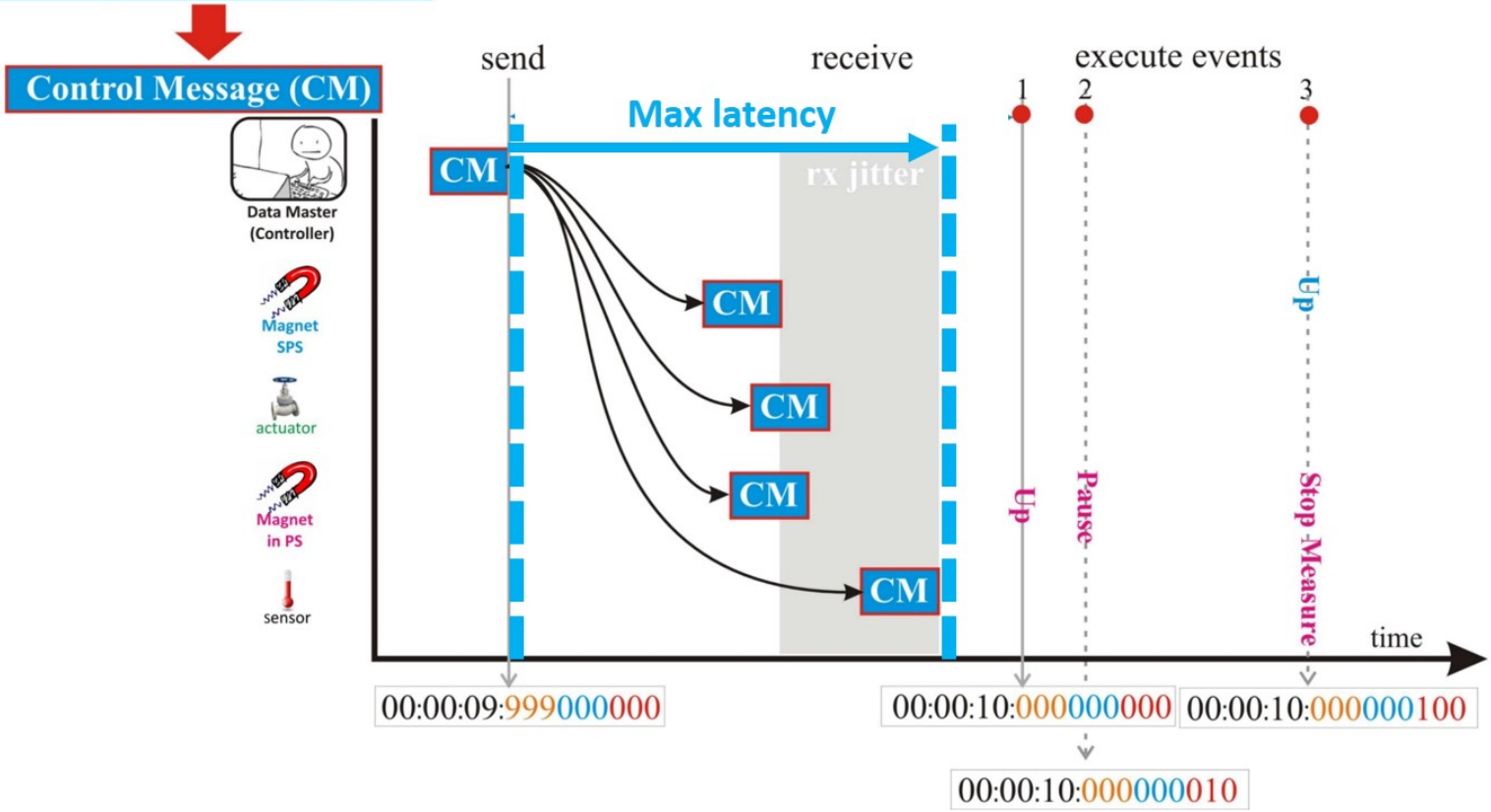


Time-based control



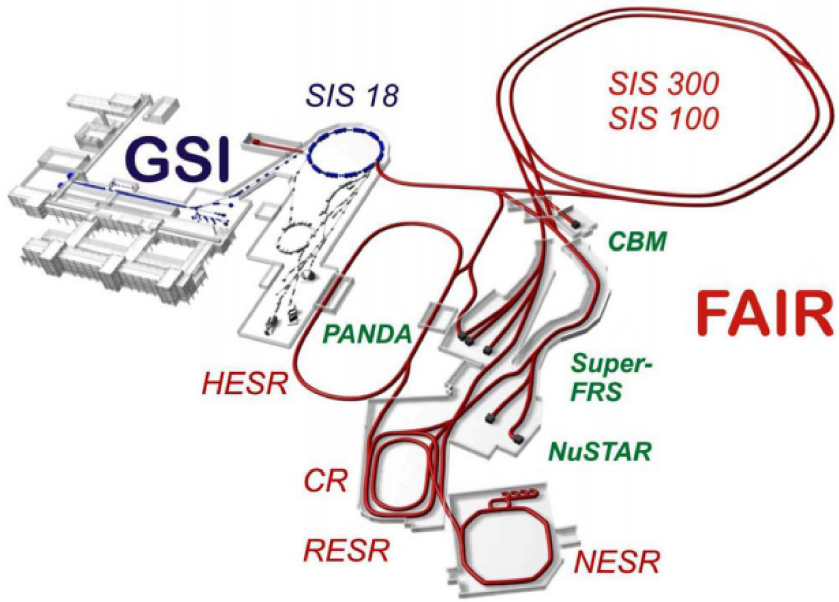
Time-based control

Event ID	Hh:mm:ss:nanoseconds
ID = 1	00:00:10:000000000
ID = 2	00:00:10:000000010
ID = 3	00:00:10:000000100



Time-based control - example application

- GSI Helmholtz Centre for Heavy Ion Research in Germany



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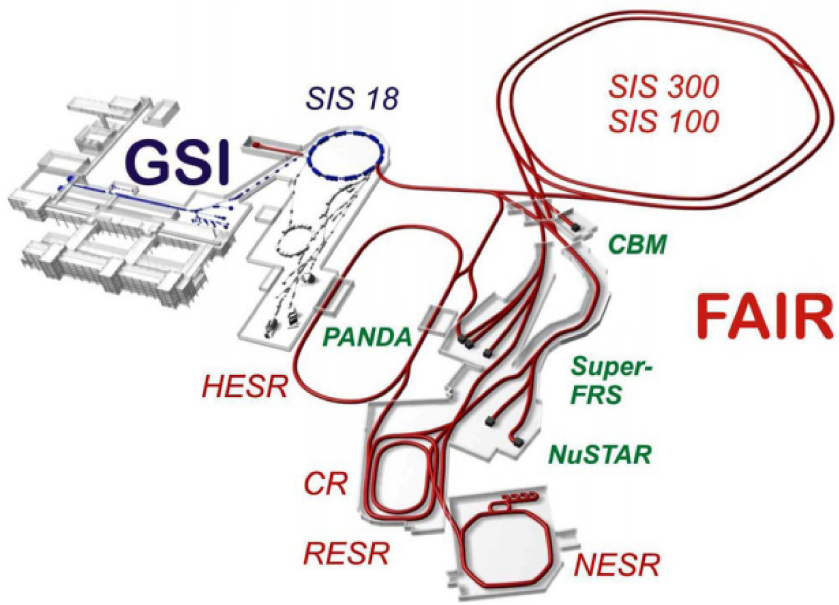
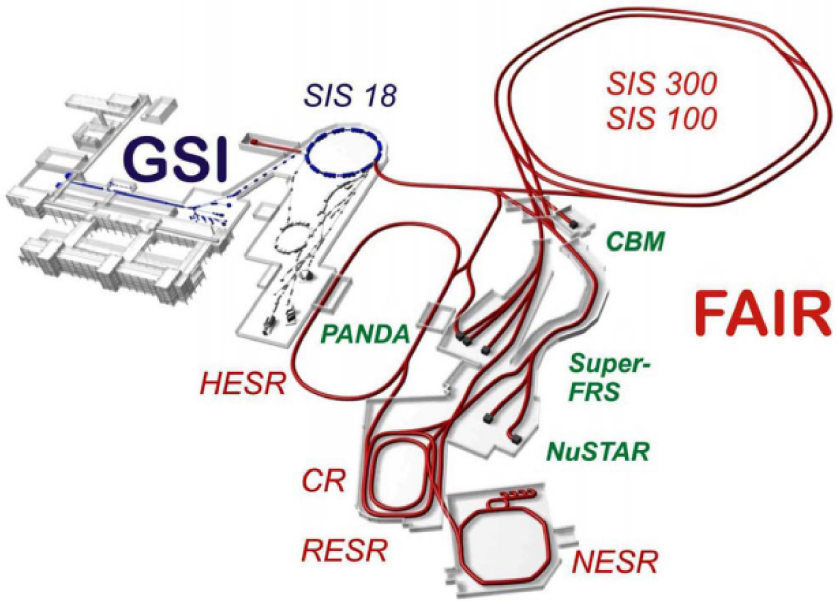


Time-based control - example application

- GSI Helmholtz Centre for Heavy Ion Research in Germany
- 1-5 ns accuracy and 10 ps precision
- WR network at GSI:
  - Operational since June 2018: 134 nodes & 32 switches
  - Final: 2000 WR nodes & 300 switches in 5 layers



Precise timestamping

- Association of time with
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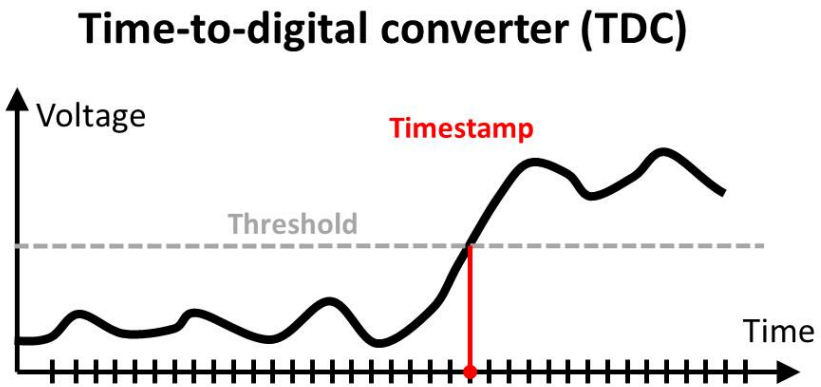
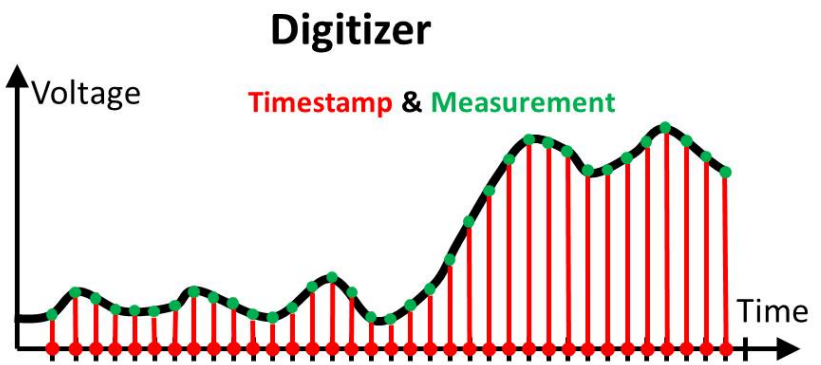
  - a sample (measured value)





Precise timestamping

- Association of time with
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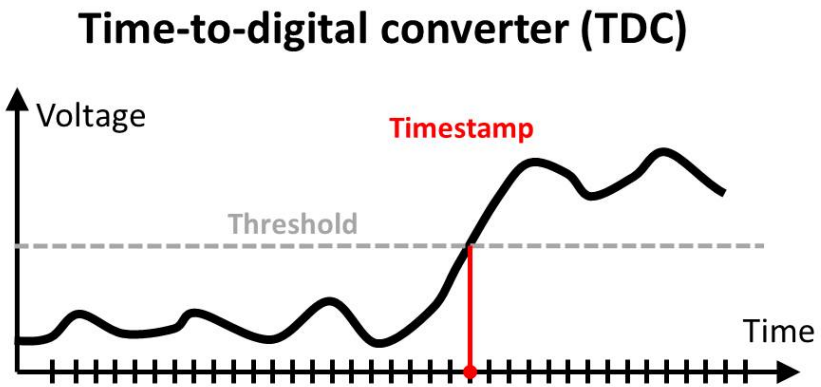
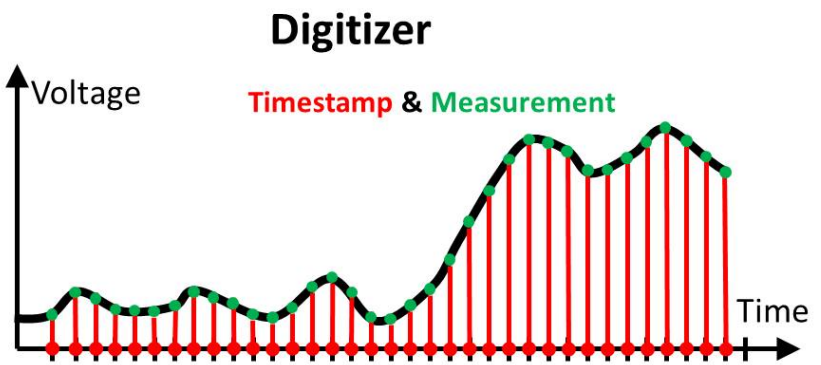
- The most widely used WR application





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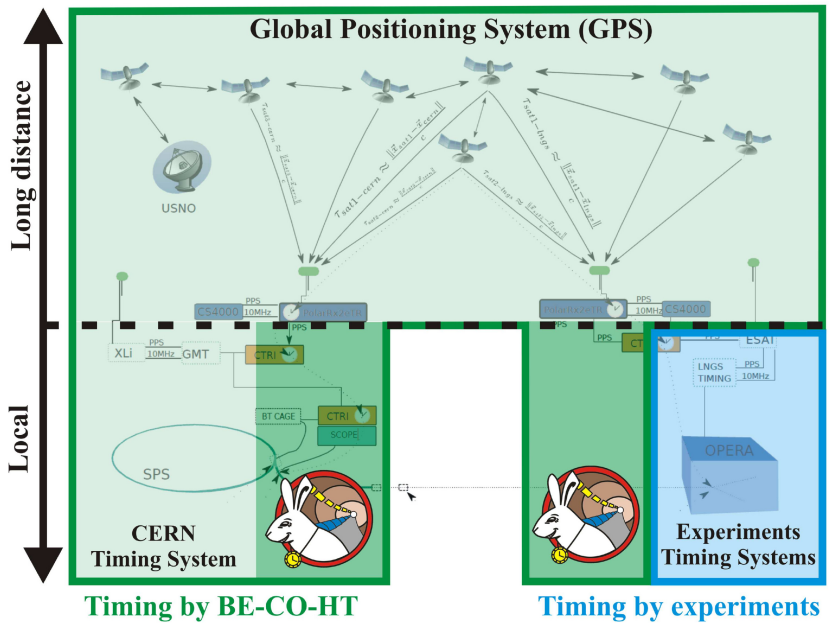
    - Speed of neutrinos - CNGS



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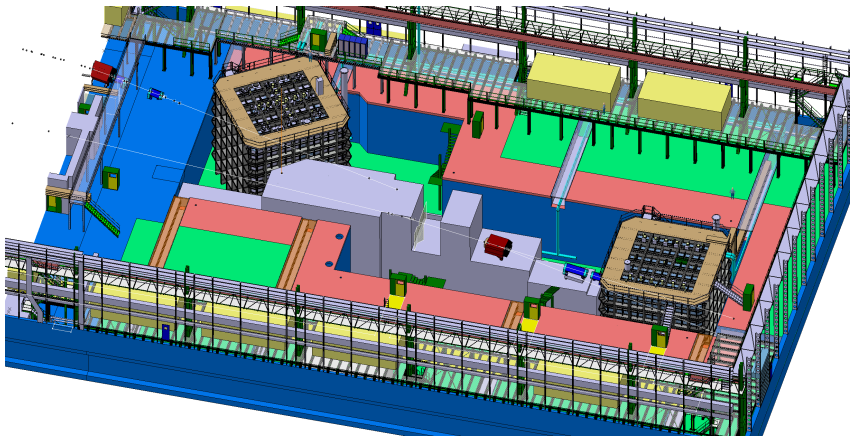

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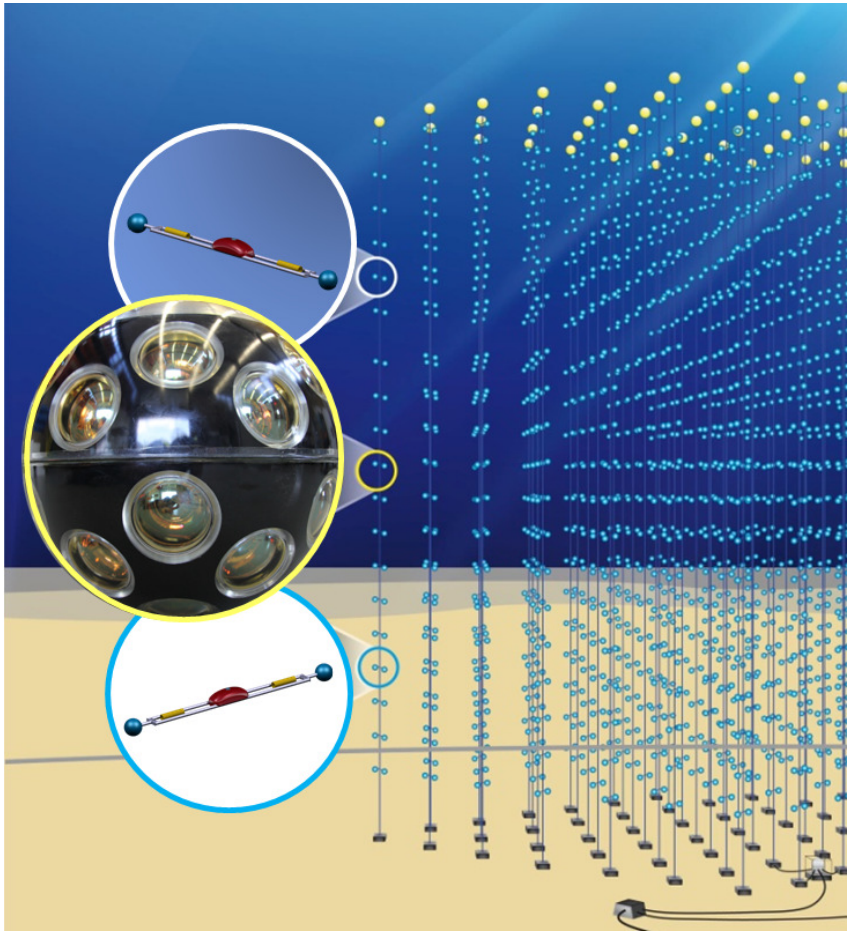

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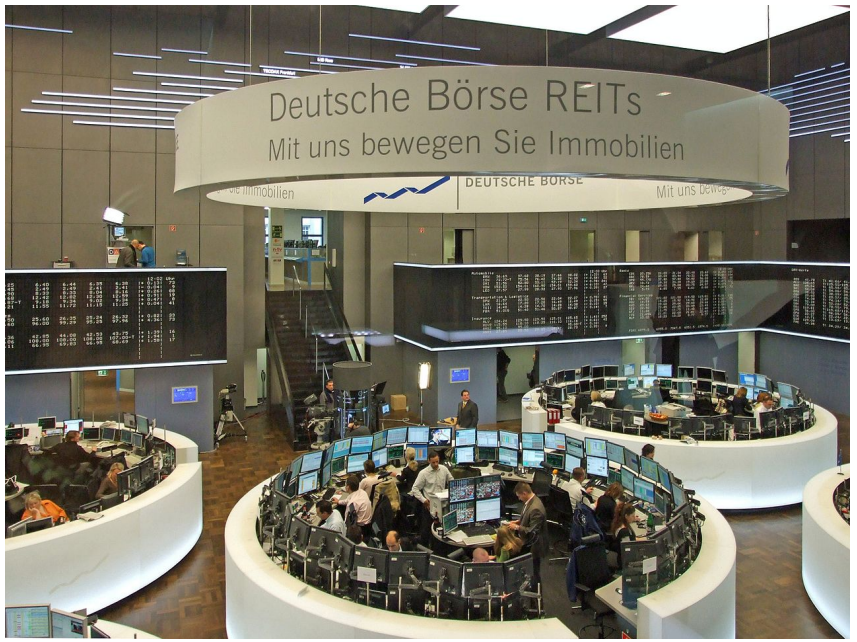
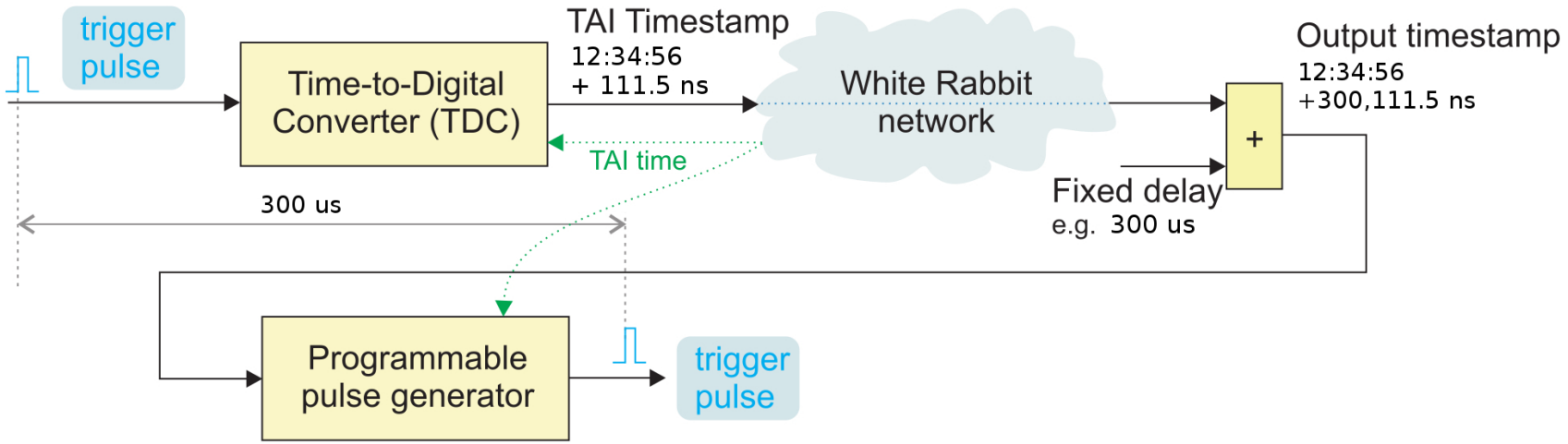
  - High Frequency Trade monitoring
    - German Stock Exchange

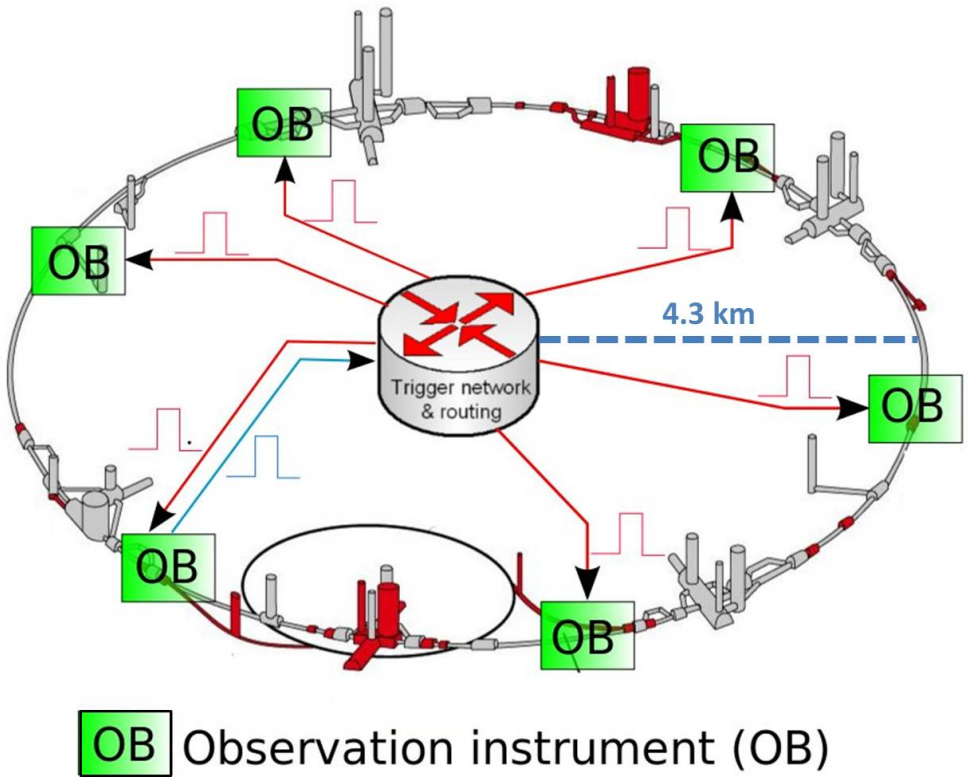


Trigger distribution



Trigger distribution - example applications

LHC trigger distribution to measure beam instabilities - since 2016



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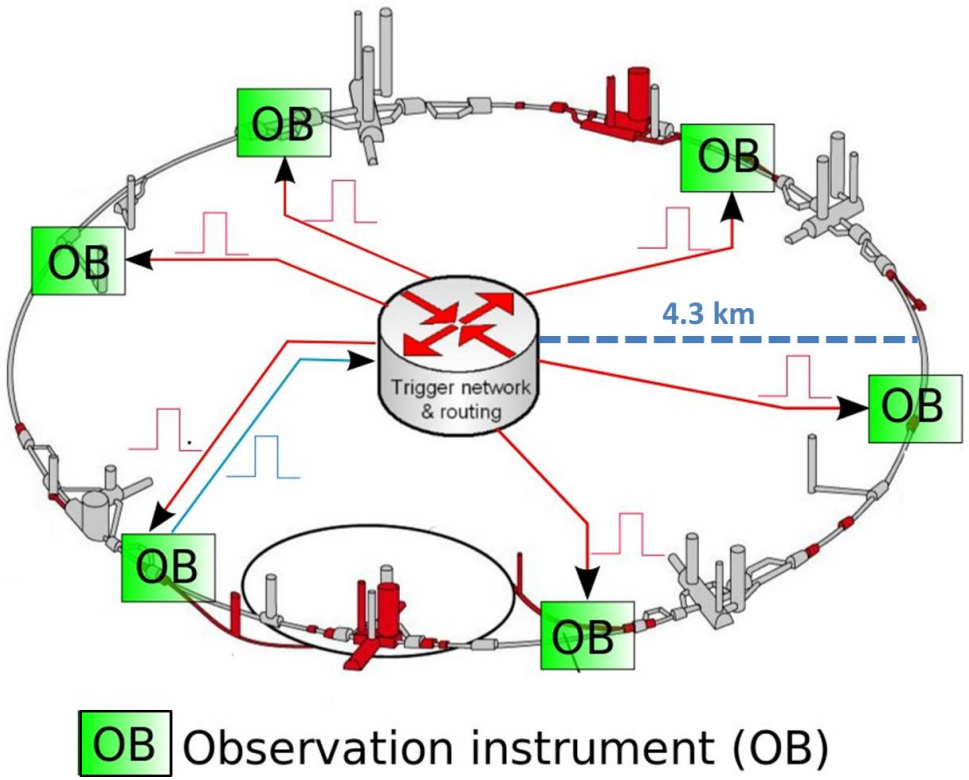
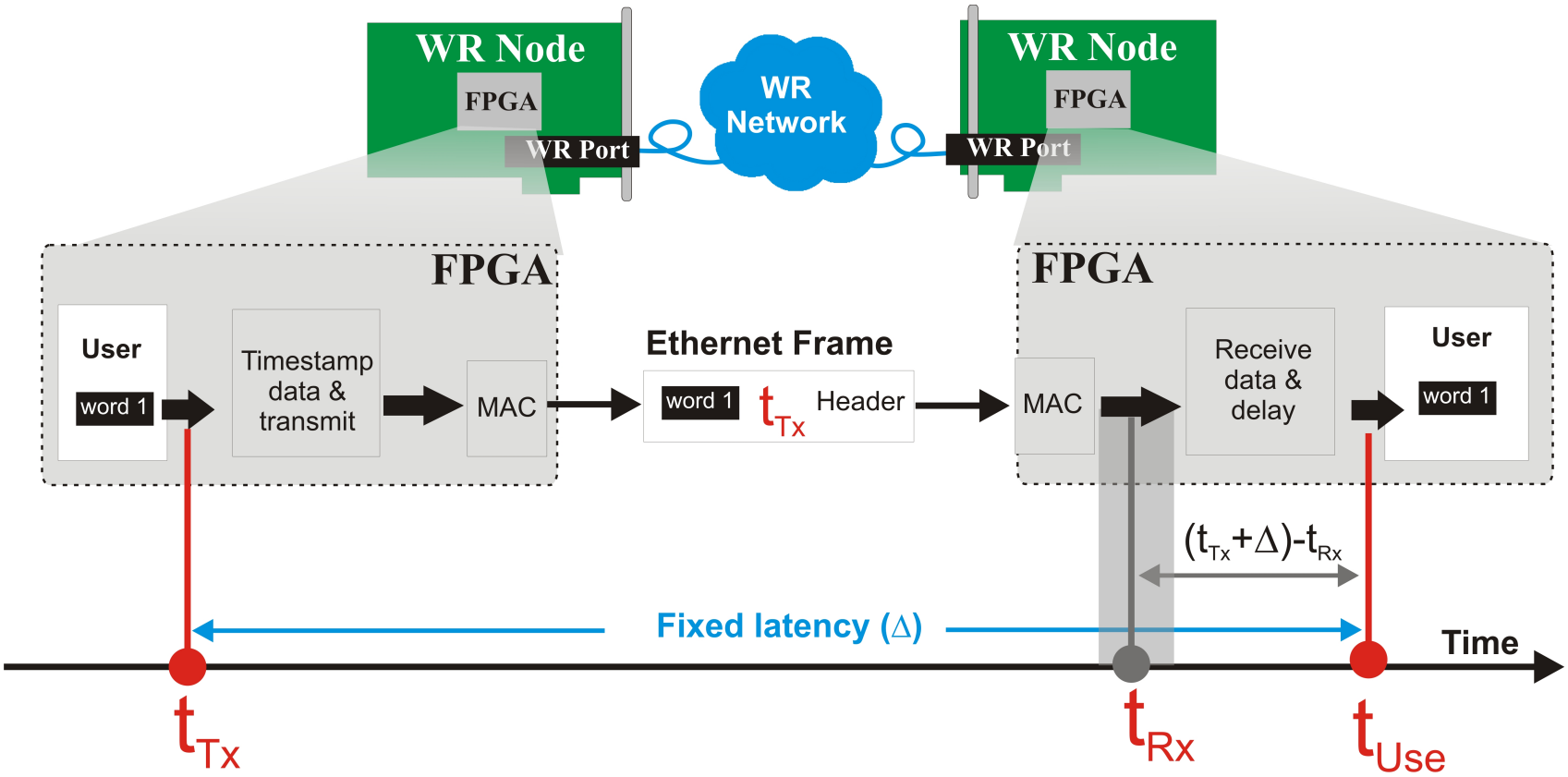


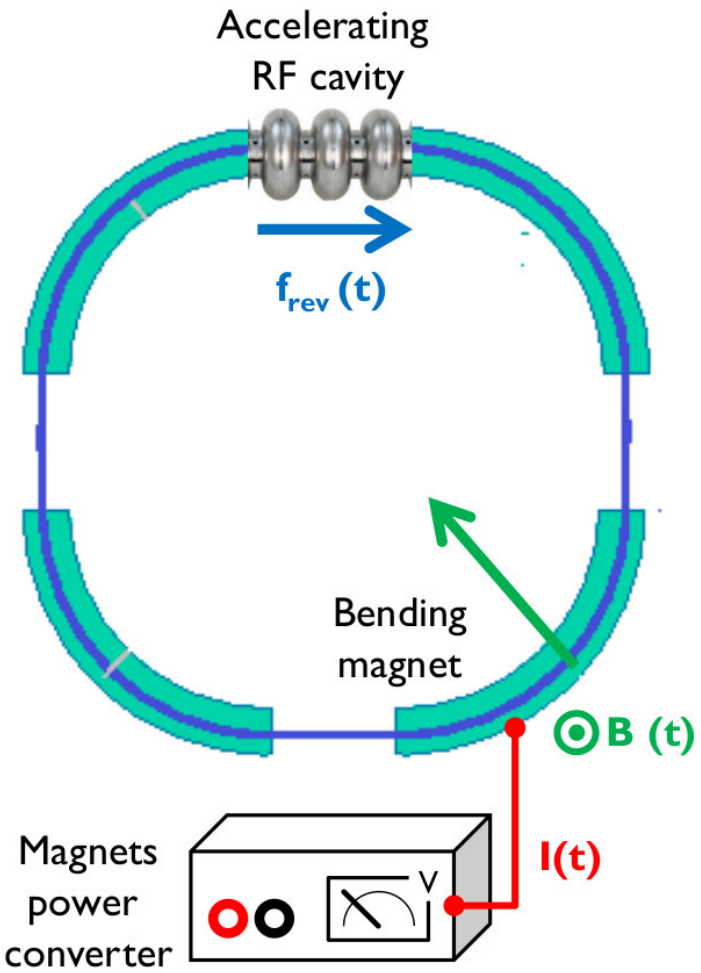
WRTD - White Rabbit Trigger Distribution- to be used for CERN's Open Analog Signals Information System (OASIS)

Fixed-latency data transfer

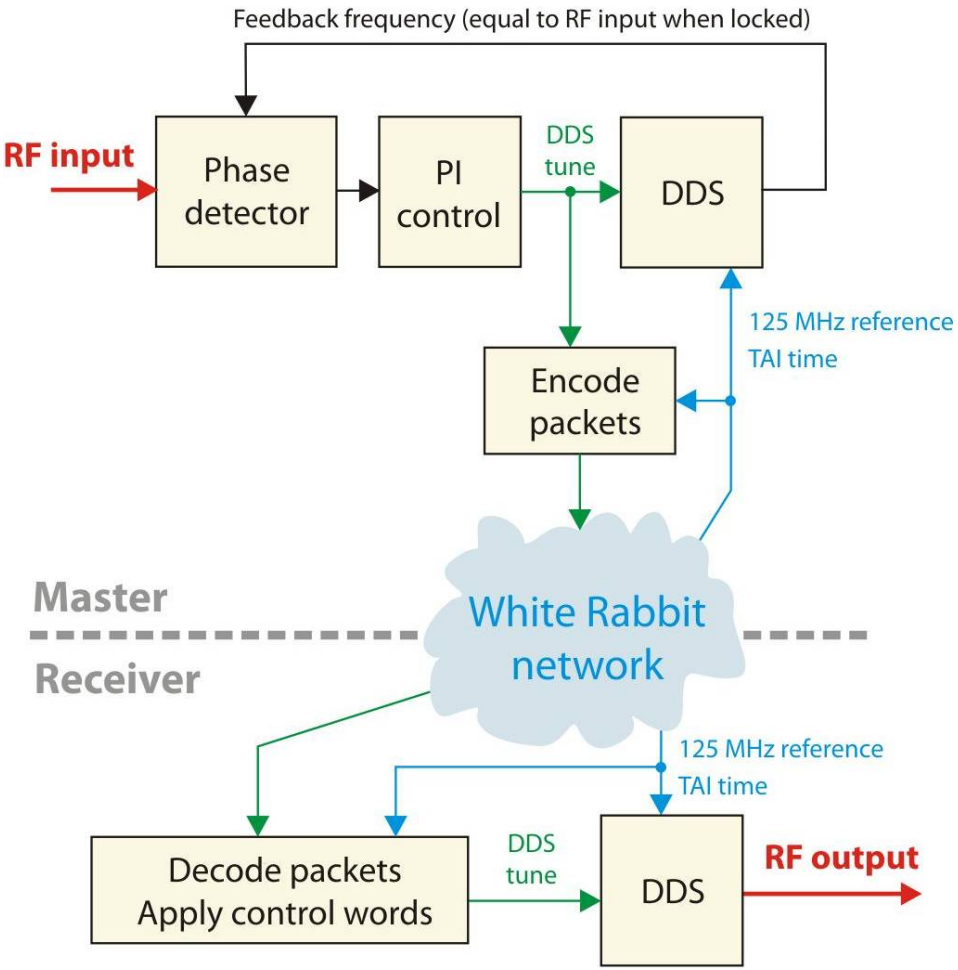


Fixed-latency data transfer- example application

Distribution of magnetic field in CERN accelerators



Radio-frequency transfer



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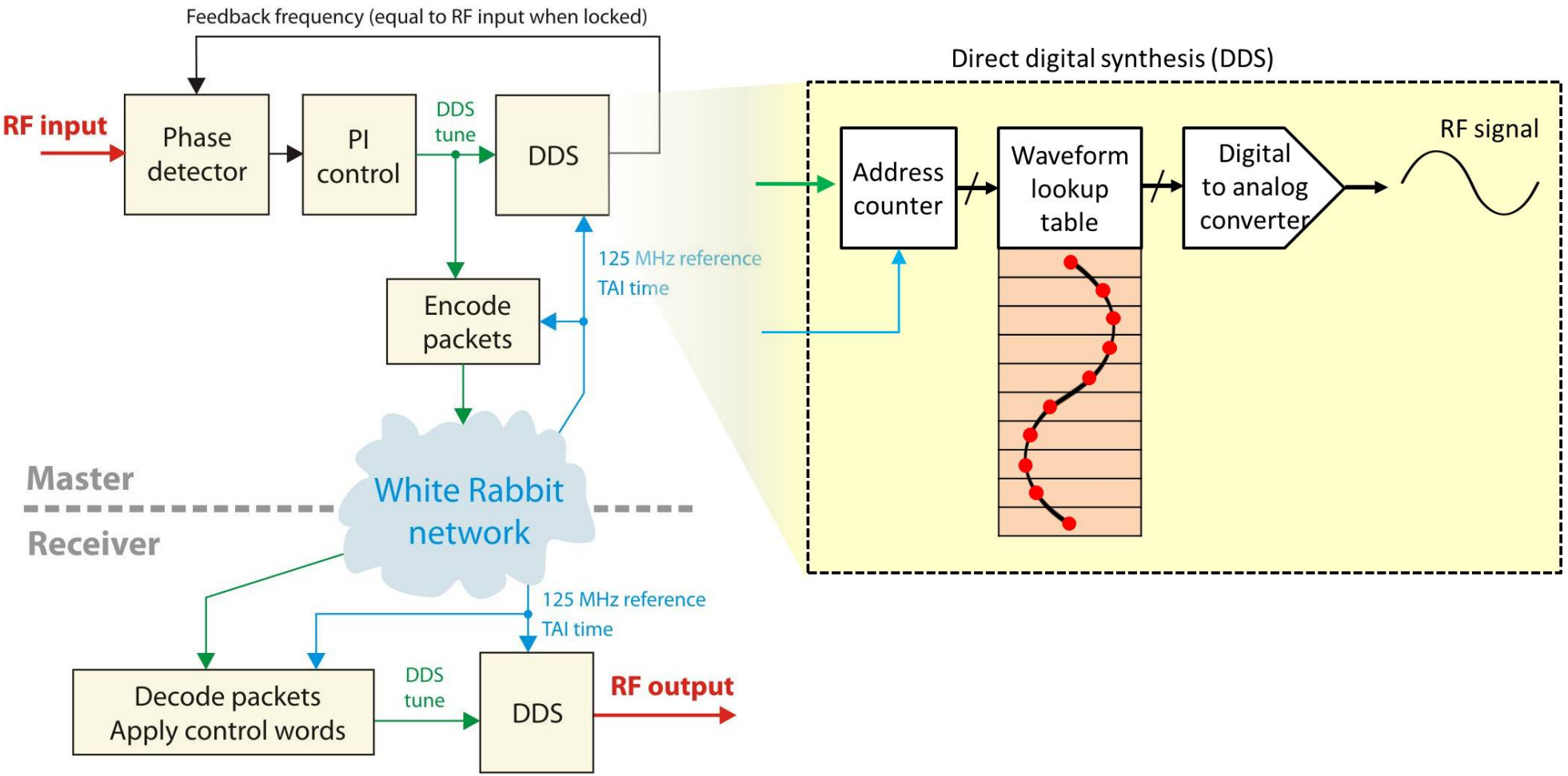

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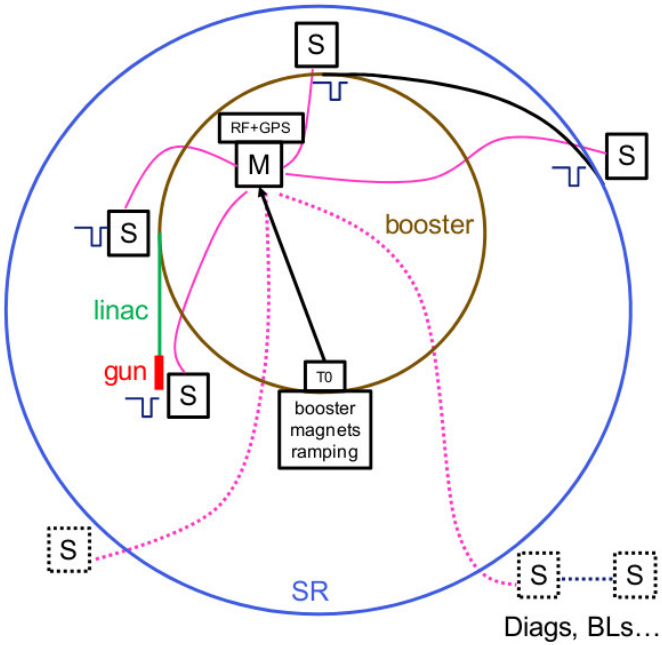

- RF over WR at European Synchrotron Radiation Facility (ESRF)
  - A prototype tested in operation: $<$10 ps jitter
- RF over WR at CERN
  - A prototype: $<$100 fs jitter and $<$10 ps reproducibility over reboots

Outline

WR standardisation in IEEE 1588 (1)

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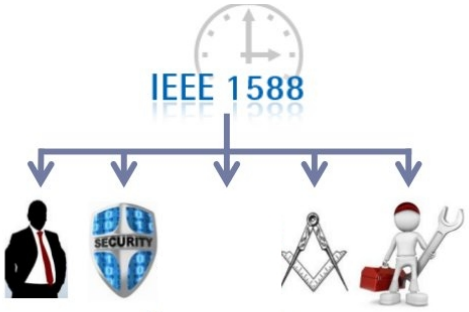

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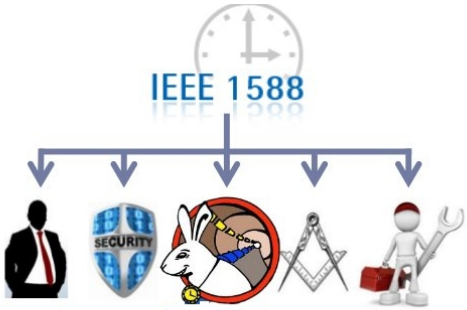

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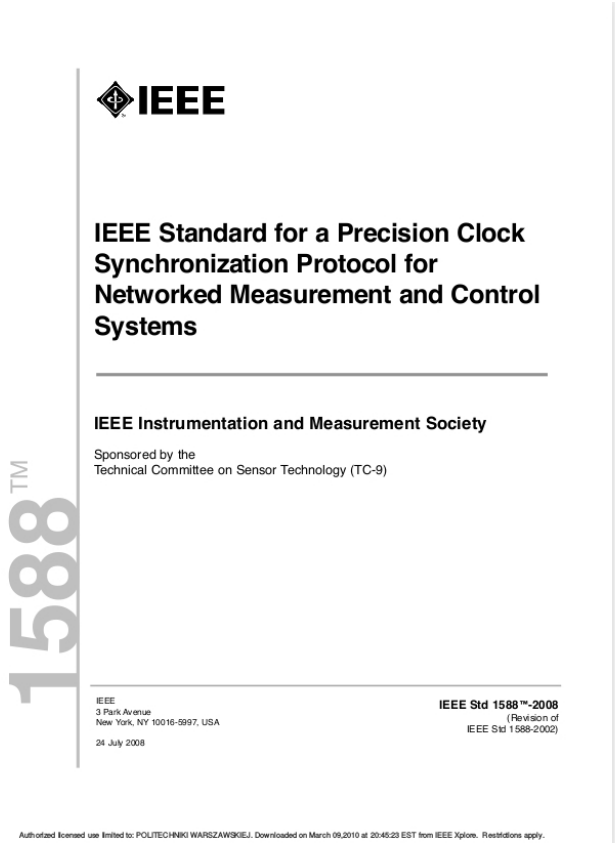
- Revised IEEE 1588 approved on 7 Nov 2019

WR standardisation in IEEE 1588 (2)



IEEE

IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

IEEE Instrumentation and Measurement Society

Sponsored by the
Technical Committee on Sensor Technology (TC-9)

1588™

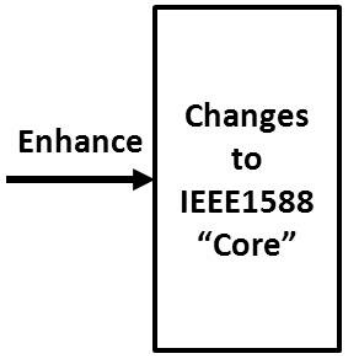
IEEE
3 Park Avenue
New York, NY 10016-5997, USA

24 July 2008

IEEE Std 1588™-2008
(Revision of
IEEE Std 1588-2002)

White Rabbit integration into IEEE 1588 as High Accuracy:
`https://www.ohwr.org/projects/wr-std/wiki/wrin1588`

WR standardisation in IEEE 1588 (2)



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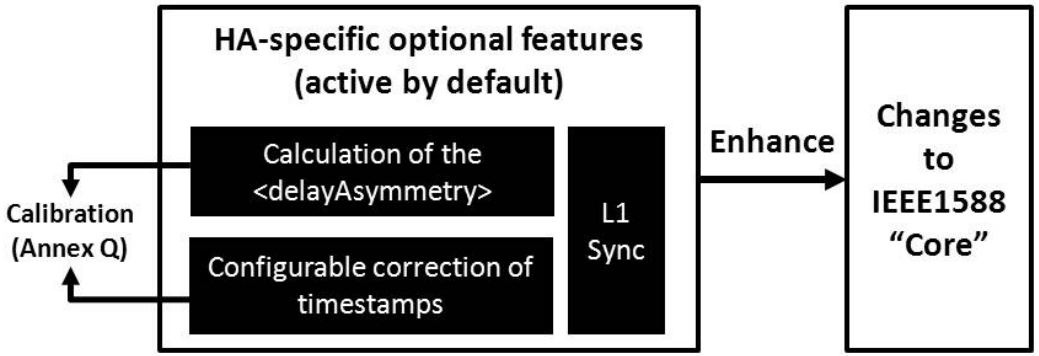

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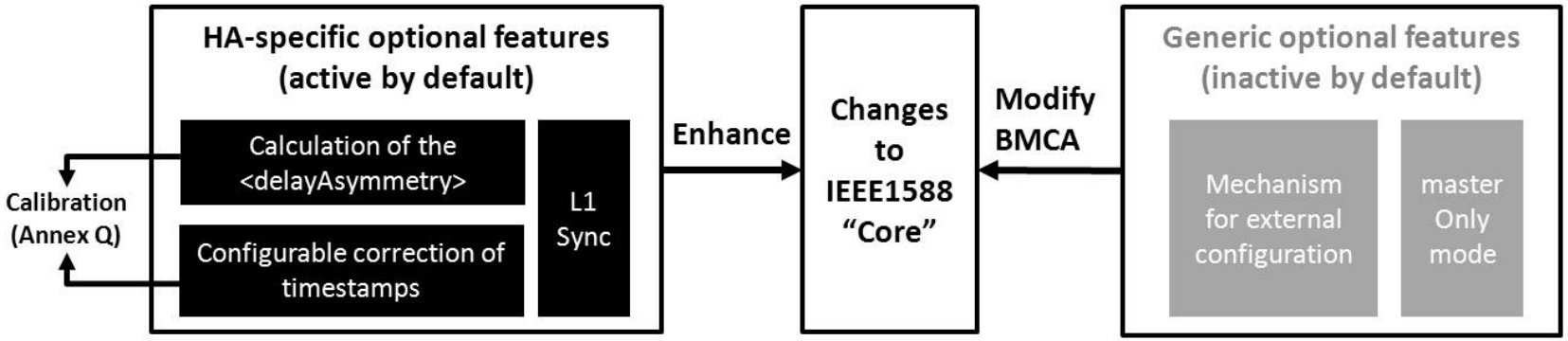

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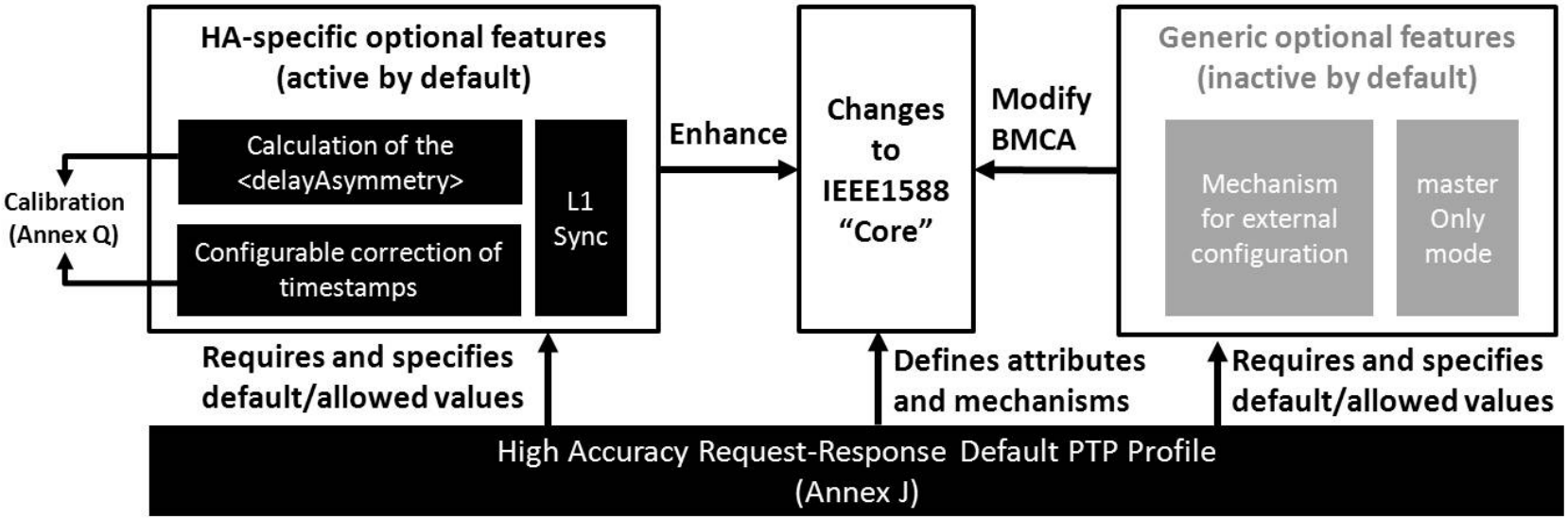

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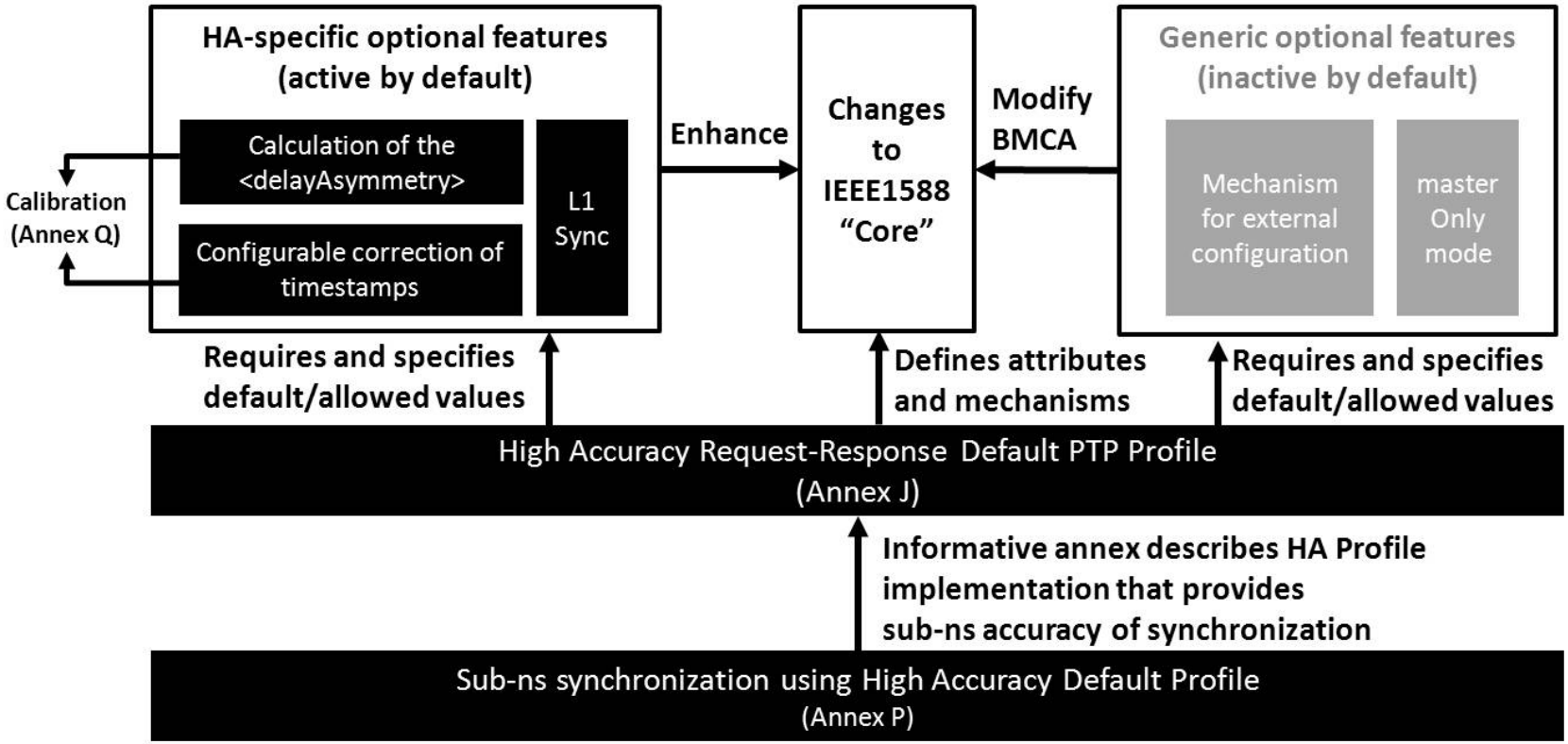

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Outline

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- Improve accuracy ($<$10 ps) and jitter ($<$100 fs)

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  (next week BE seminar)

Outline

Summary

- Ethernet-based synchronization

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- Showcase of technology transfer

Q&A

Questions?

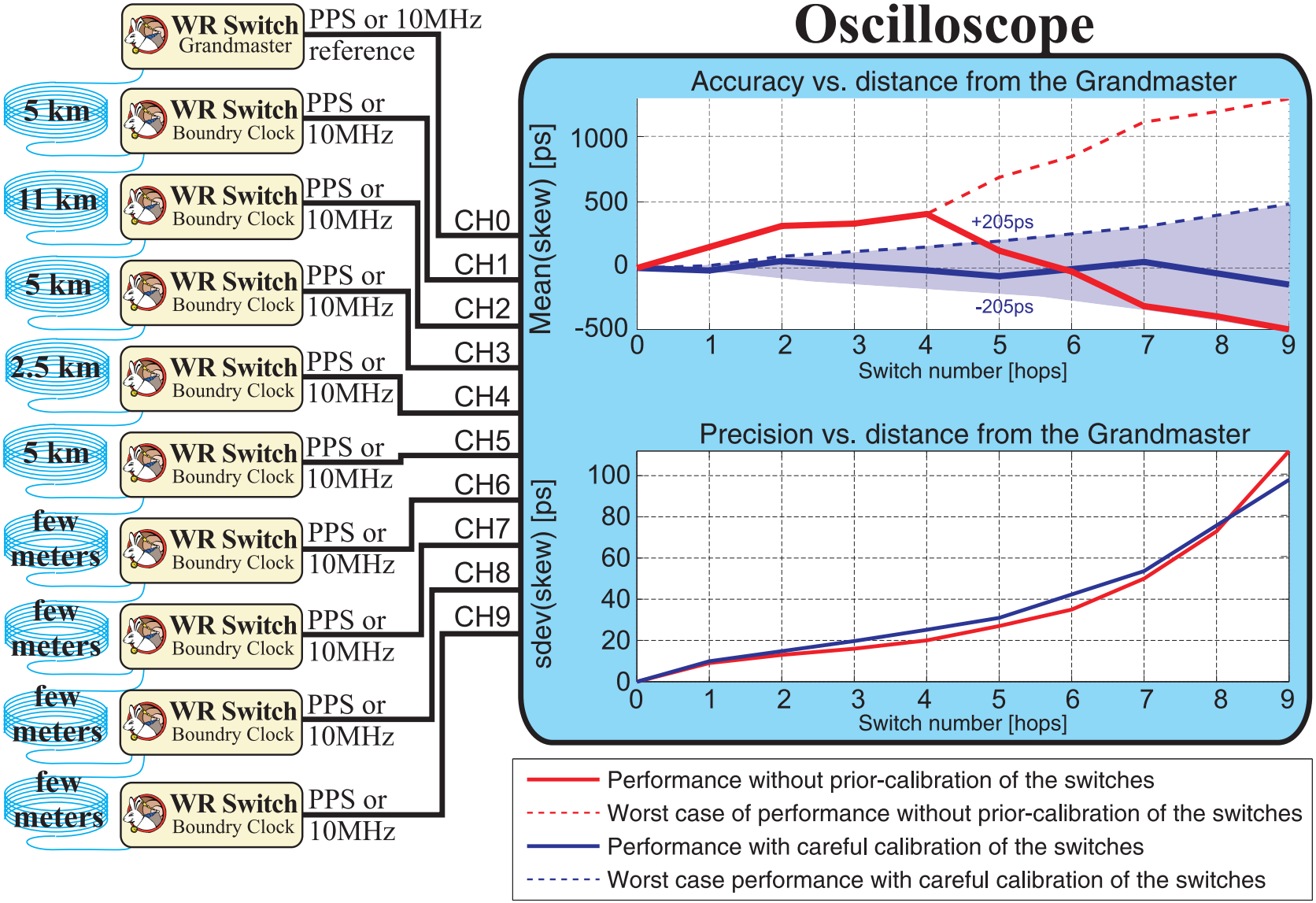
WR Project page: http://www.ohwr.org/projects/white-rabbit/wiki

Backup slides

Backup slides

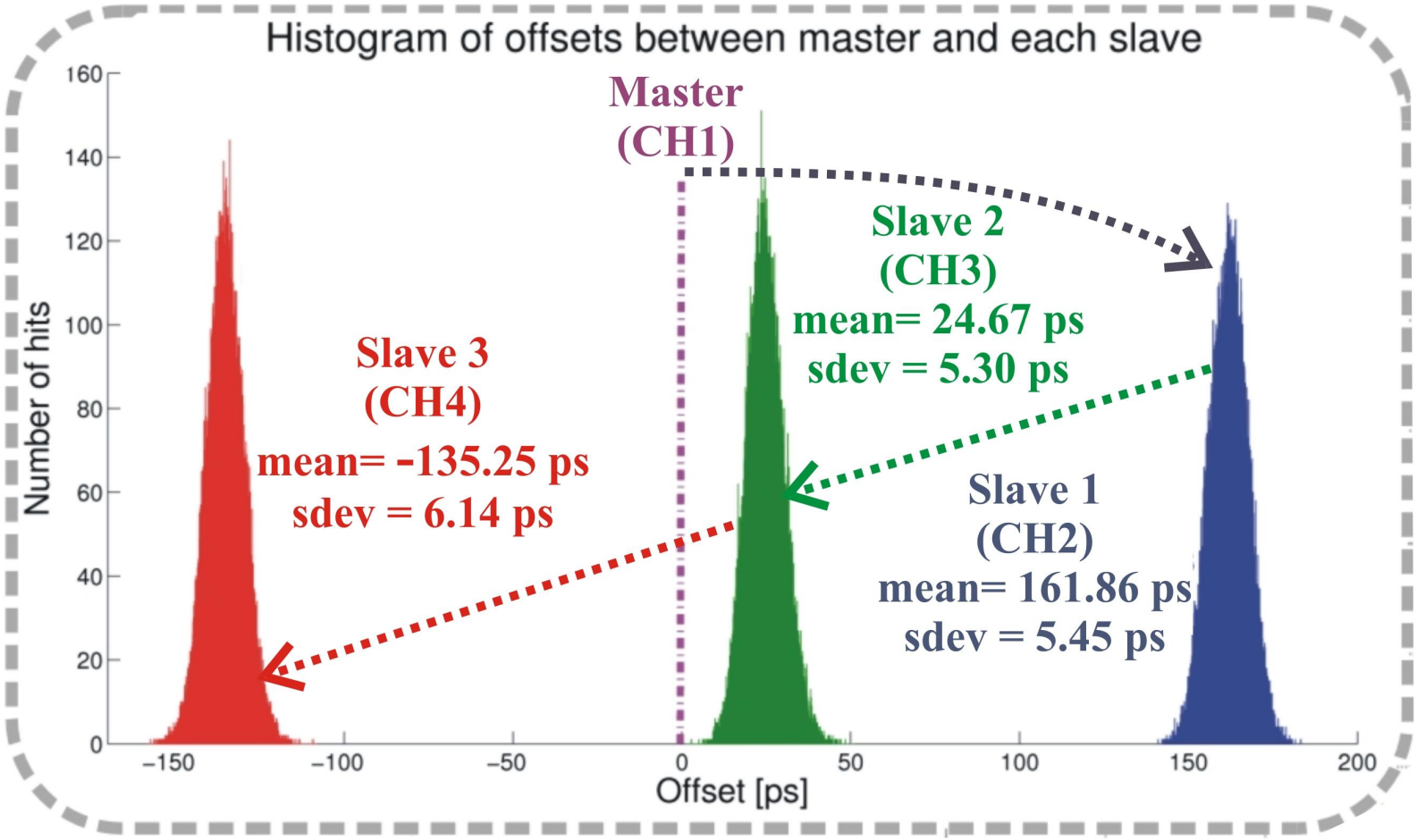
Outline

WR performance in a long chain



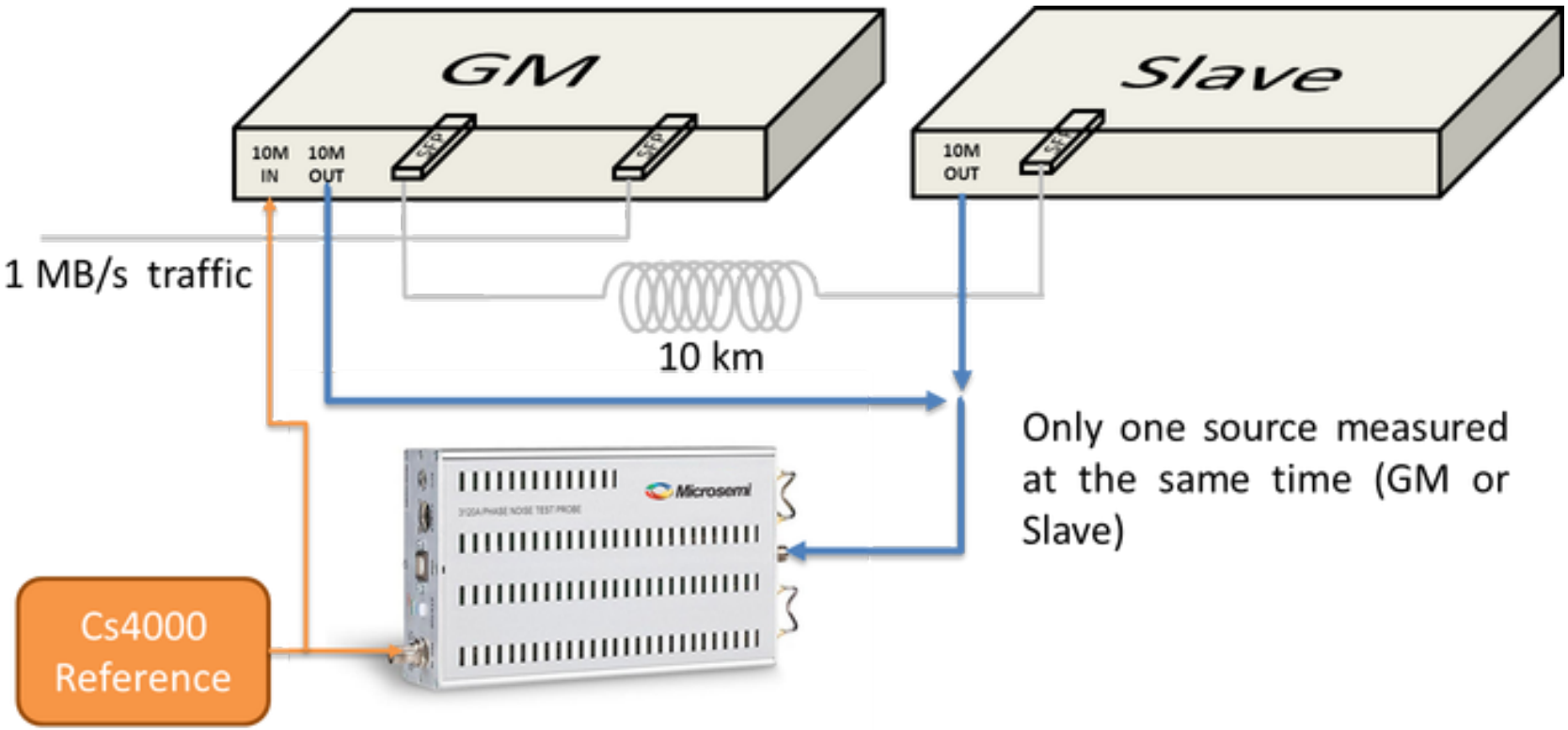
Outline

Time transfer: out-of-the-box



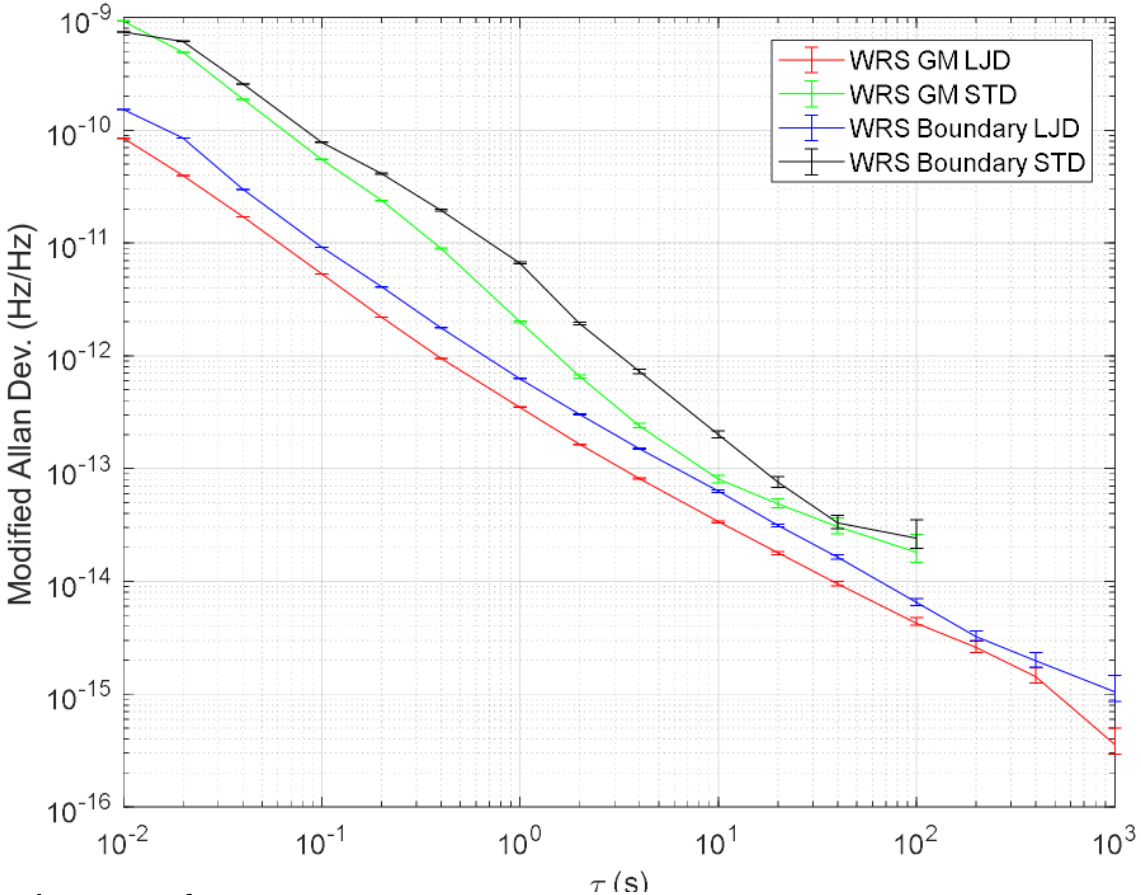
Reported in 2011

Frequency transfer: out-of-the-box and improved



Measurement device: Microsemi/Microchip 3120A Phase Noise Test Probe

Frequency transfer: out-of-the-box and improved



- Out-of-the-box performance:
  - **GM-in to GM-out**: jitter of **9 ps** RMS 1 Hz–100 kHz and MDEV of **2E-12** τ=1 s ENBW 50 Hz
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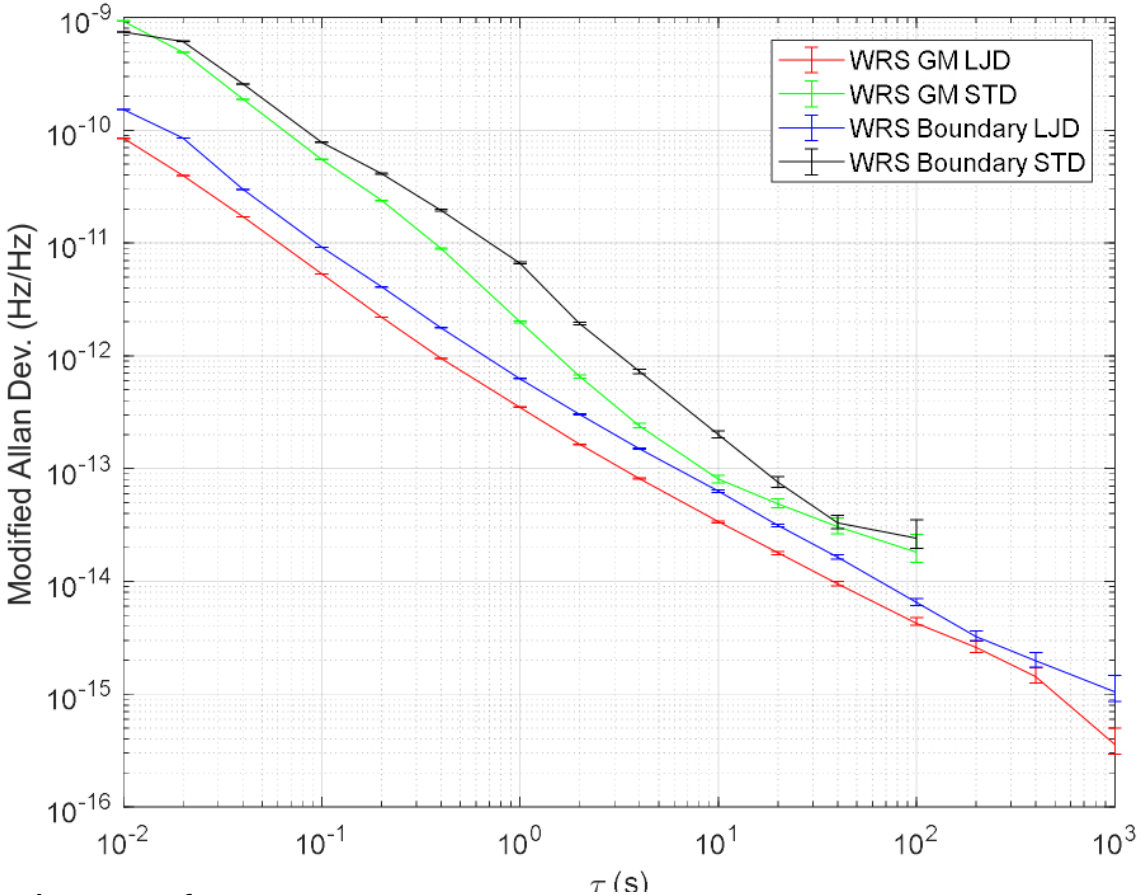

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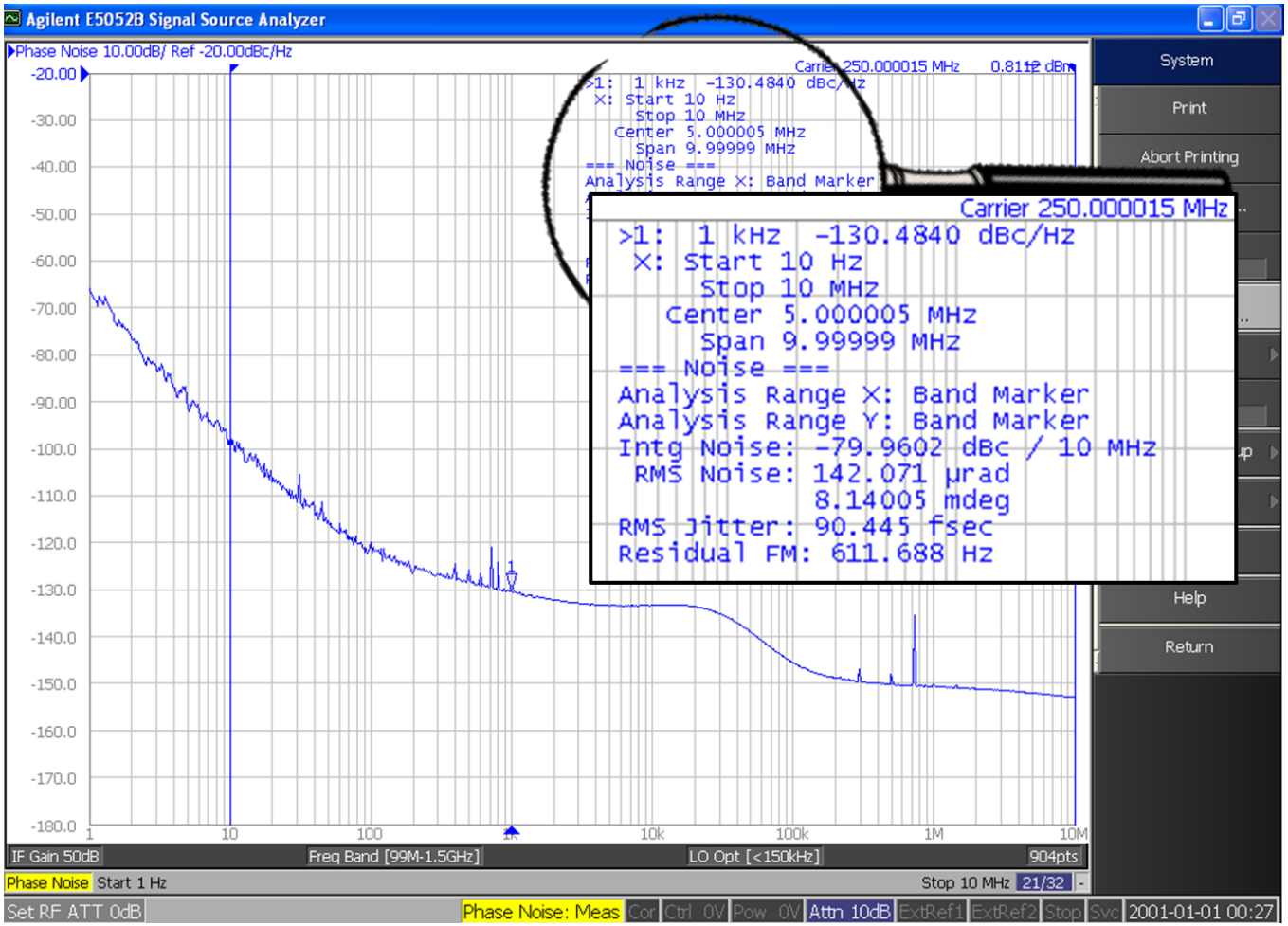
- WR Switches improved with Low Jitter Daughterboard (LJD):
  - **GM-in to GM-out**: jitter of **1 ps** RMS 1 Hz–100 kHz and MDEV of $<$**5E-13** τ=1 s ENBW 50 Hz
  - **GM-in to Slave-out**: jitter of $<$**2 ps** RMS 1 Hz–100 kHz and MDEV of $<$**7E-13** τ=1 s ENBW 50 Hz

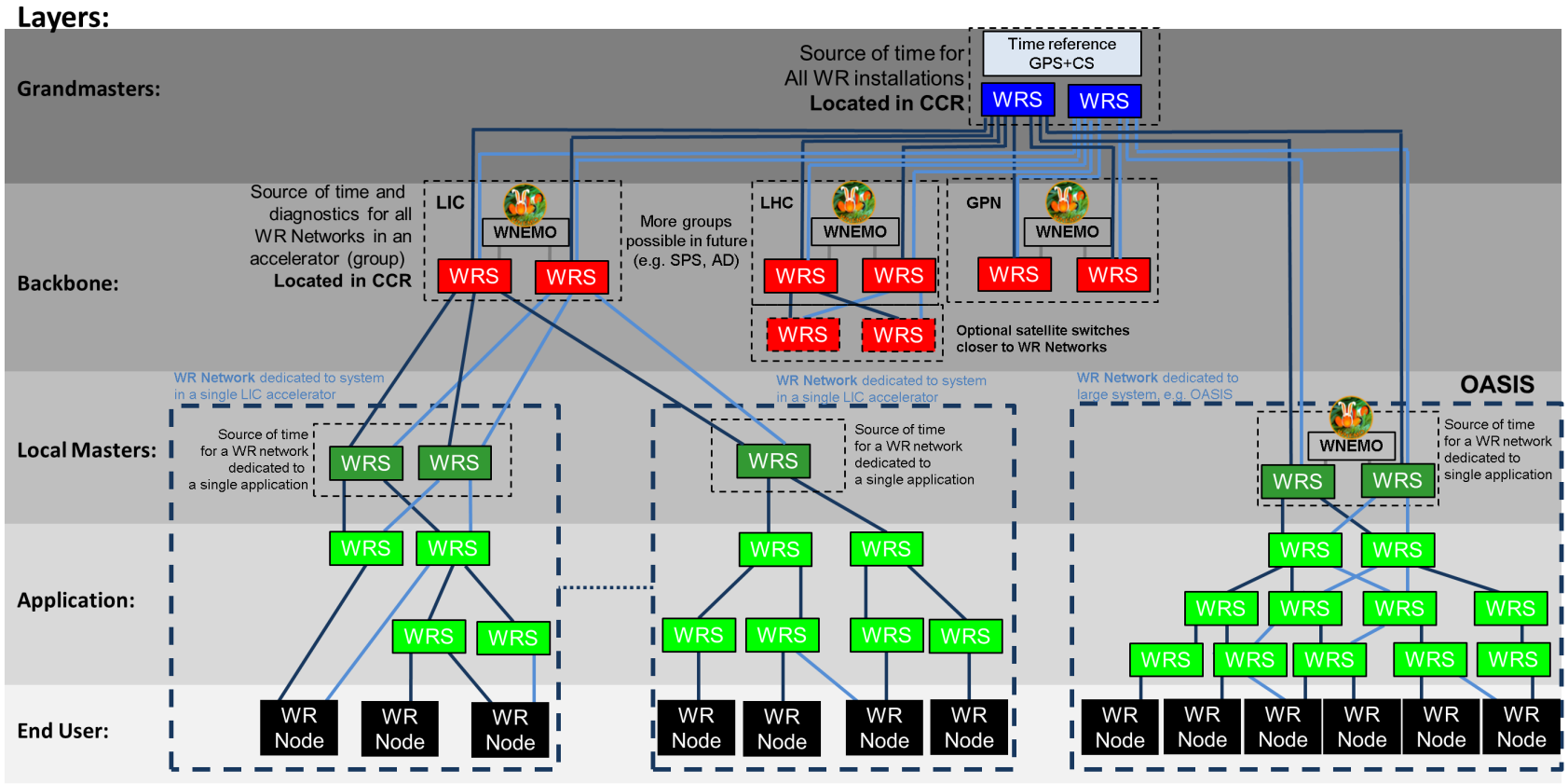
WR time & frequency tranfser: state of the art



- **GM-out to end-node-out**: accuracy of $<$**10 ps**
- **GM-out to end-node-out**: jitter of $<$**100 fs** RMS 10 Hz–10 MHz

Outline

Global WR network at CERN



WRS WRS WRS — WR Switch

Active fiber Ethernet link

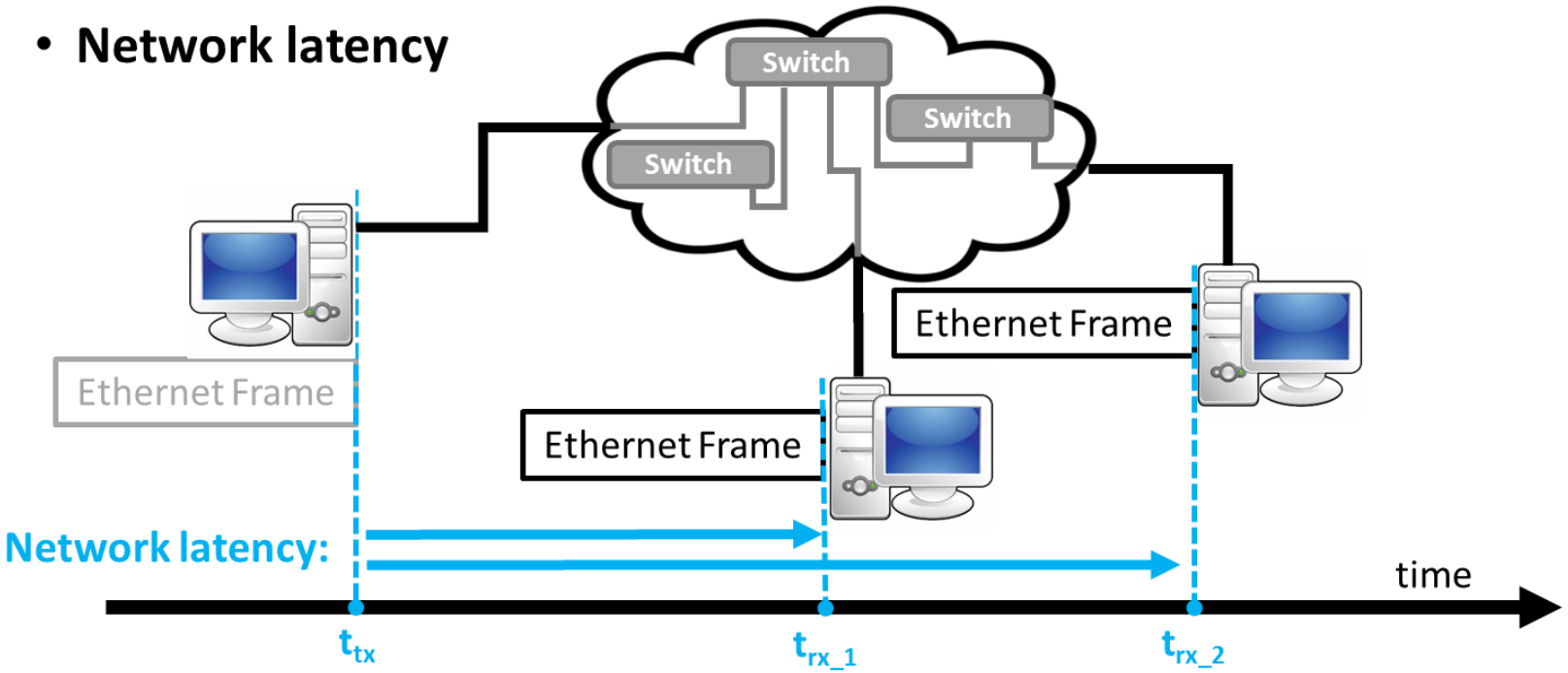
Backup fiber Ethernet link

Copper Ethernet link

Outline

Determinism and Network Latency

- **Determinism**
  A deterministic system is predictable: it provides calculable and consistent characteristics of operation that are required by the application, e.g. **network latency** of data transmission.
- **Network latency**

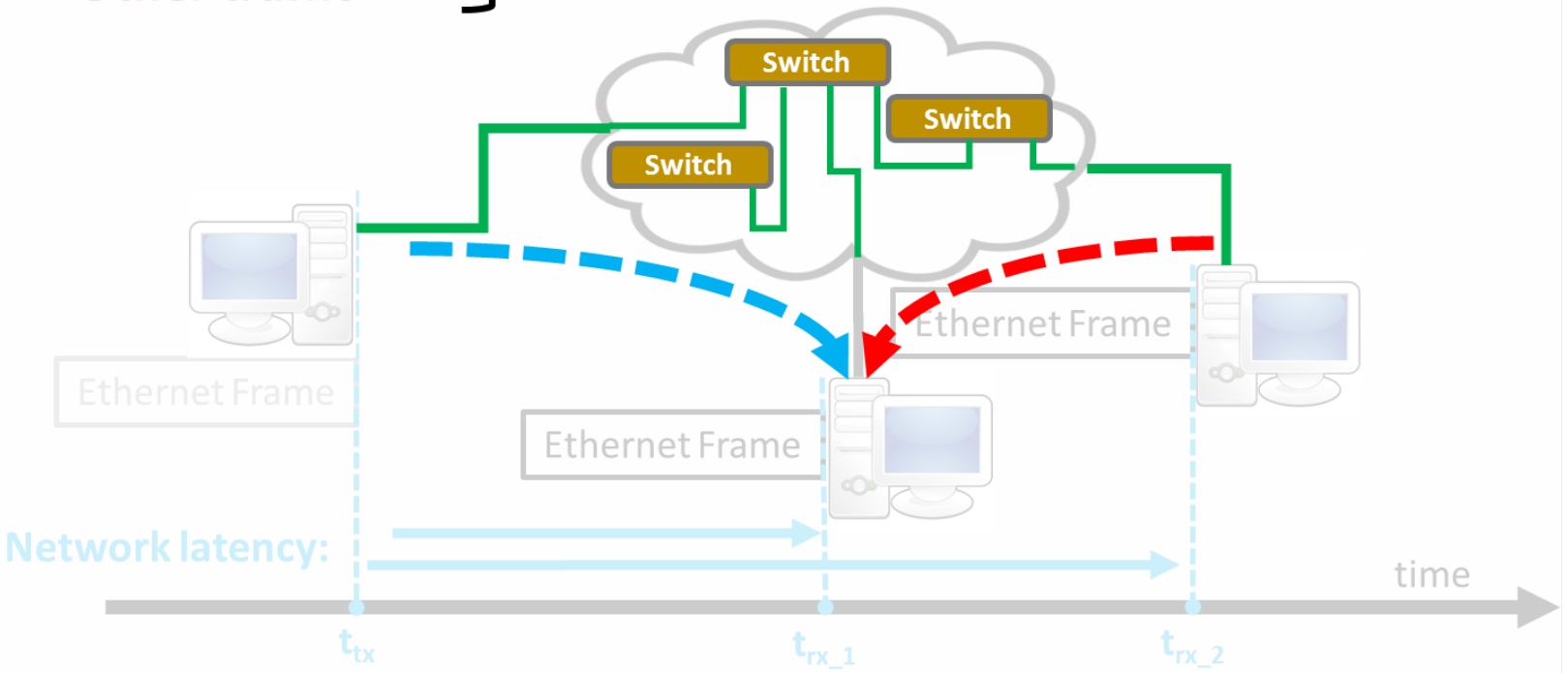


Deterministic network is a network in which we can calculate the maximum latency

Network Latency Contributors

- Cables: 5us/km – we cannot do much about this
- Switch operation
- Other traffic

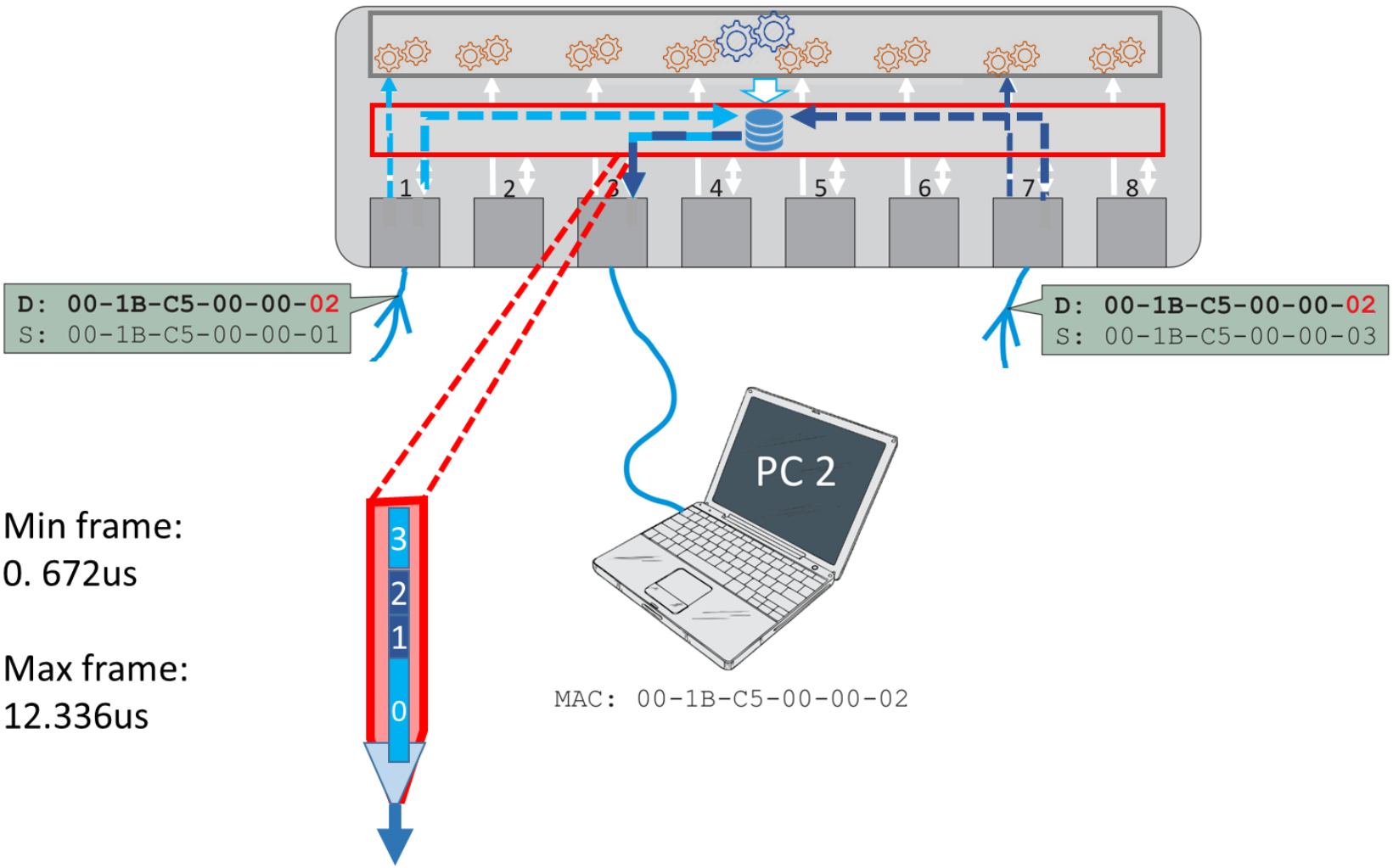
We can do something about this



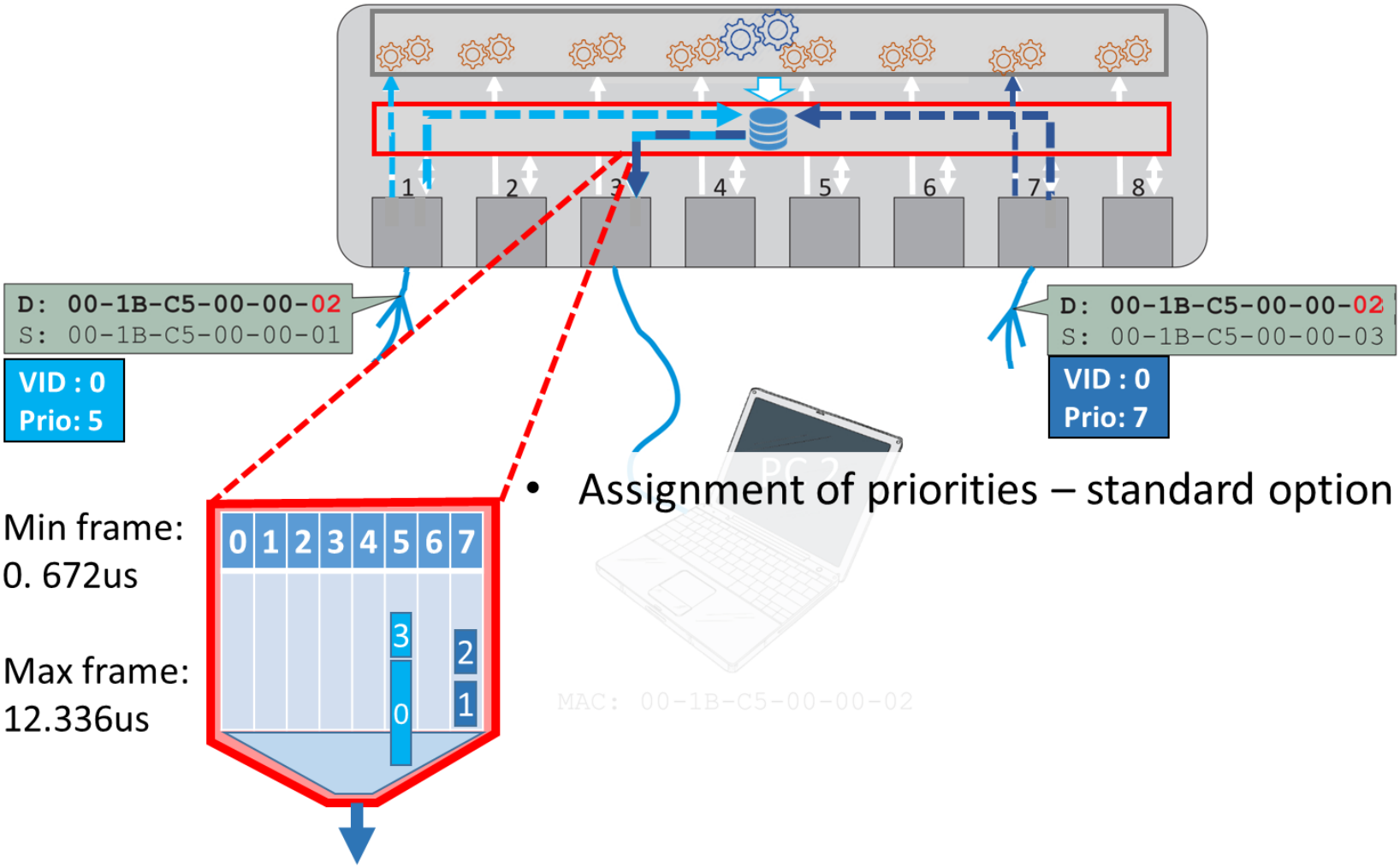
Determinism in WR

- ”White Box” design of WR switch - allows thorough analysis
- Backward-compatible extension of the IEEE 802.1Q std

Priorities

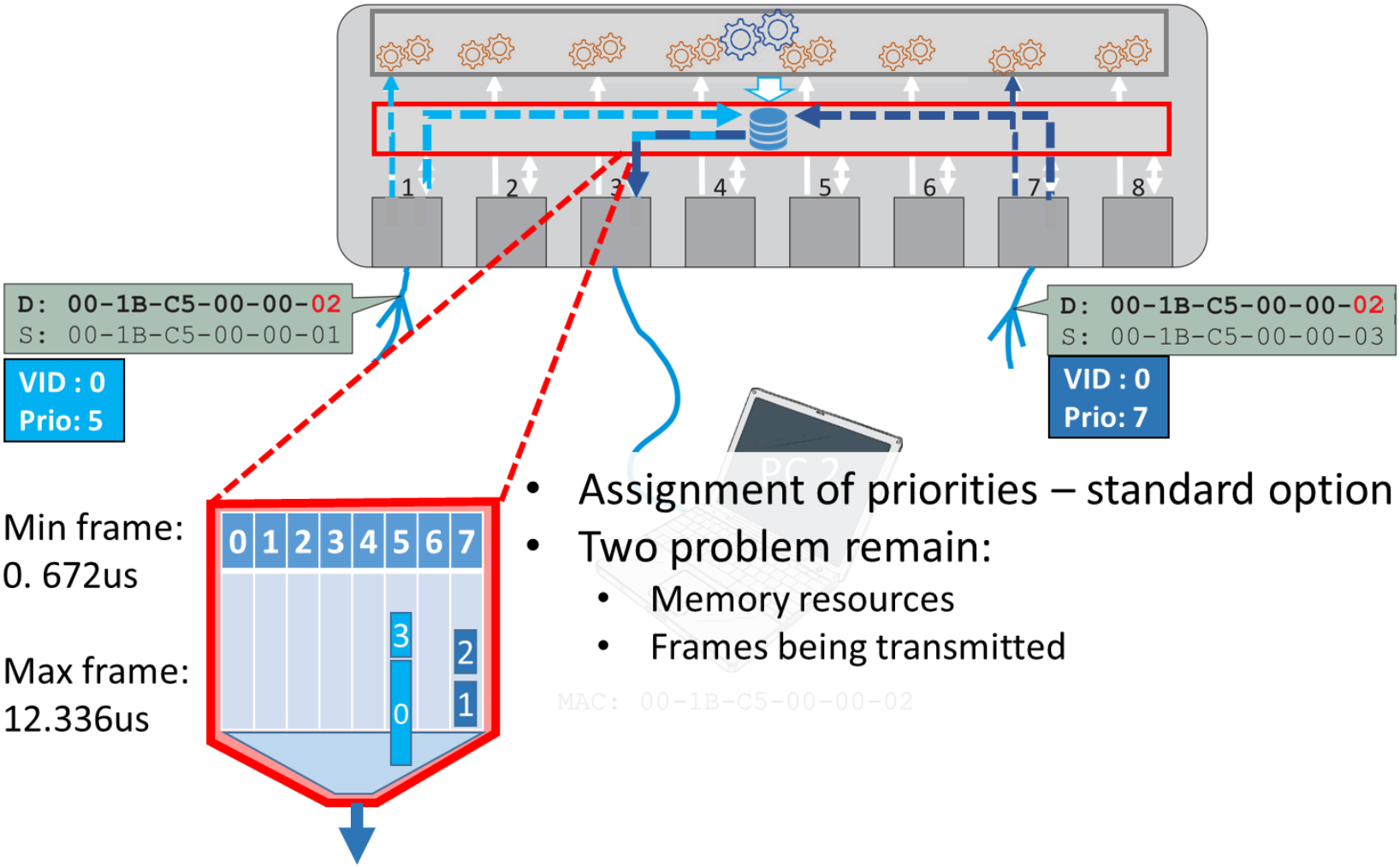

1
2
3
4
5
6
7
8
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-03
PC 2
MAC: 00-1B-C5-00-00-02
3
2
1
0
Min frame:
0. 672us
Max frame:
12.336us

Priorities

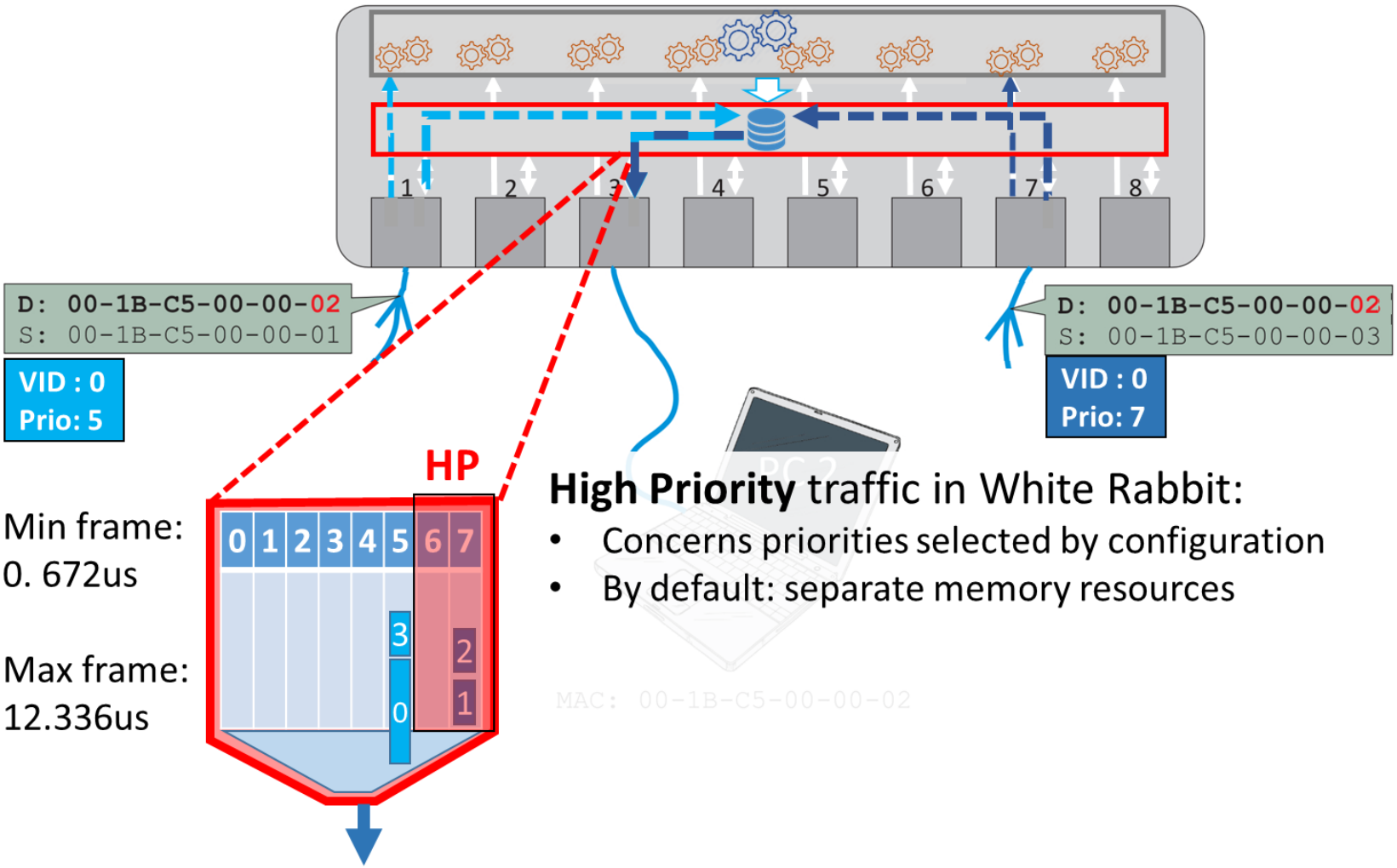


- Assignment of priorities – standard option

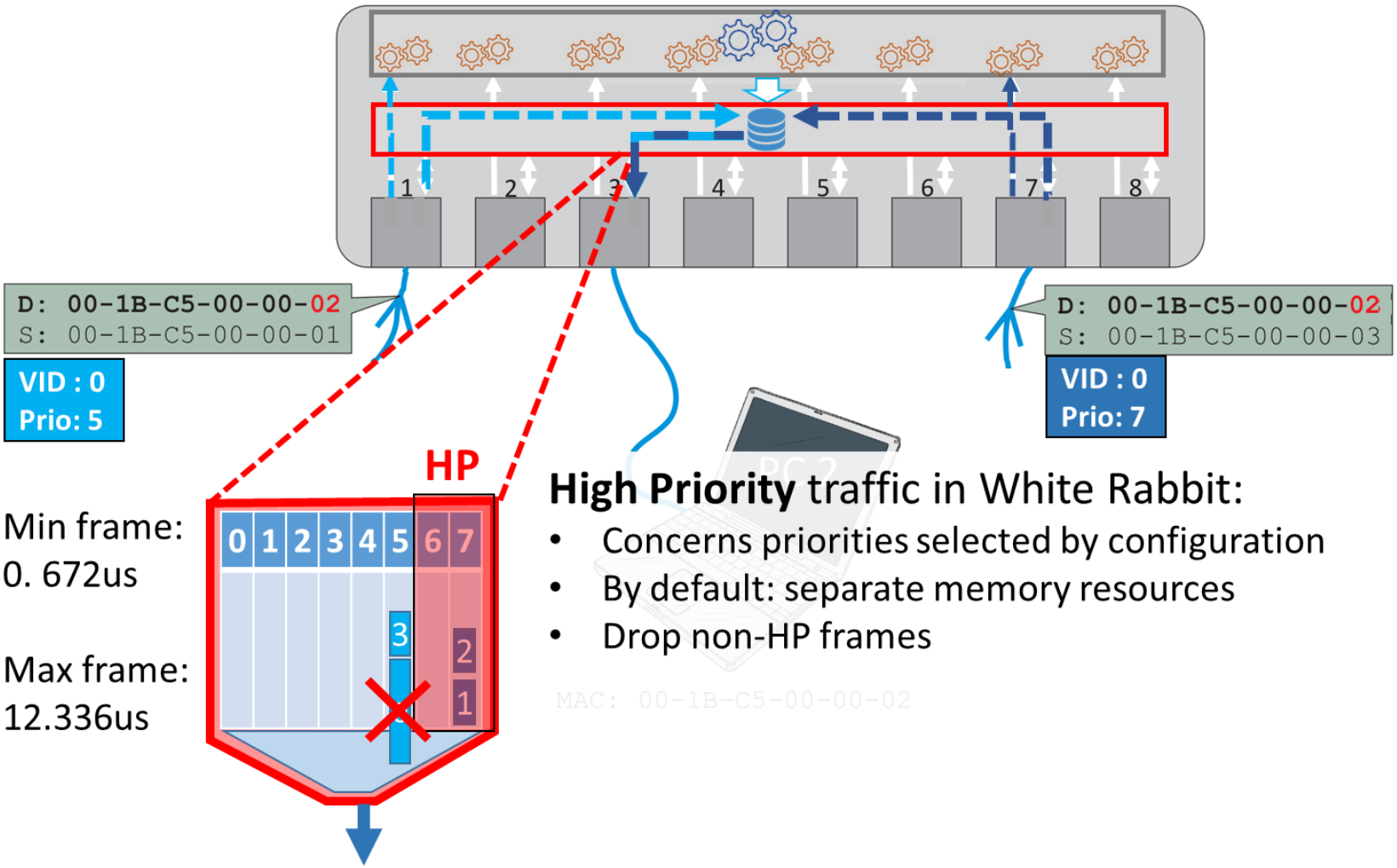
Priorities


1
2
3
4
5
6
7
8
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01
VID : 0
Prio: 5
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-03
VID : 0
Prio: 7
Min frame:
0. 672us
Max frame:
12.336us
0 1 2 3 4 5 6 7
3
2
0
1
• Assignment of priorities – standard option
• Two problem remain:
• Memory resources
• Frames being transmitted

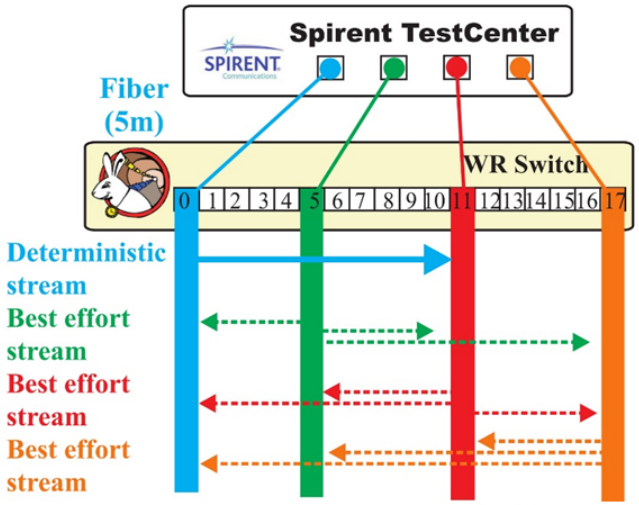
High Priority



High Priority



WR Switch Latency



Intervening traffic	Latency [us]			
	One switch		Two switches	
	Max	Pk-pk	Max	Pk-pk
No	3.1	0.3	5.8	0.5
WR-PTP	5.6	2.8	8.7	3.9
Non-HP traffic	3.1	0.2	N/A	N/A