Maciej Lipiński

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Electronics engineer with experience in controls, data acquisition and high-precision synchronisation systems, as well as scalable systems for precise measurement of position. Developer of HDL for FPGA-based electronics and software for embedded devices. Leader and manager of projects involving diverse stakeholders and users, including industry. Co-author, lead standardiser and developer of White Rabbit (WR) technology, with responsibilities for the CERN-wide WR network architecture, as well as its integration, deployment, maintenance and operational support of WR for critical systems. CERN representative to IEEE, ITU-T and SNIA standardisation bodies. Organiser of international conferences, meetings and workshops. CERN guide and Open Days volunteer.

Professional Experience

CERN:	**Electronics Engineer Staff, Fellow, PJAS & Doctoral Student**, BE-CEM-EDL
2010 - today Switzerland	

- **Manager of projects** crossing different CERN groups and fields of expertise, as well as involving industrial partners, coupling CERN-specific and industry-oriented applications to benefit the Organization and maximise dissemination, 15+ projects, 0.85 MCHF total budget.
- **Technical leader** in developments of hardware (PCB design), gateware (FPGA design) and software (embedded and real-time with/without OS), supervising and coordinating internal and external developments.
- **Supervisor and mentor** of students, fellows as well as experienced staff members (5 in total).
- **Gateware developer** (VHDL and SystemVerilog) for complex FPGA-based electronics used in critical systems of controls infrastructure and equipment groups, such as BTrain and SPS LLRF, including modeling, simulations, implementation, testing.
- **Software developer** for embedded Linux WR switch and DI/OT System Board, OS-less PTP Core, and real-time software implementation of Phase-Locked Loop.
- **Network designer** responsible for the architecture, operational guidelines, configuration and maintenance of the CERN-wide WR network with high availability requirements.
- **Commissioning and operational first-line support** for the CERN-wide WR network, and attached critical WR-systems: BTrain in PSB/PS/SPS/LEIR/AD/ELENA, LLRF in SPS.
- **Expert in synchronisation** based on clock signal distribution at the physical layer, coupled with packet-based exchange of timestamps, to provide sub-ns alignment of timing signals.
- **Expert in reliability** for mission-critical systems; developed a comprehensive design for a CERN-wide highly reliable next-generation control and timing network.
- **Initiator and driving force of strategic initiatives**, such as the WR standardisation in IEEE 1588 and the WR Collaboration.
- **Quality assurance** through compliance, functional and performance tests, and design reviews.
- **Technology disseminator** sharing knowledge with world-leading engineers internally (working-groups, forums and informal meetings), and as a representative to IEEE, ITU-T, SNIA, invited speaker at multiple conferences and workshops.
- **Main organiser** of international events at CERN with 50-100+ participants, as well as social events for colleagues.
- **Author of multiple documents and publications (see Annex)**, including the WR Specification, substantial parts of the IEEE 1588-2019 standard, conference, magazine and journal articles, WR trainings and multiple presentations.

SAMSUNG:	**Junior Software Engineer**, Samsung Electronics Research and Development Centre
2009 - 2010 Poland	Software developer (C++) of a graphical user interface for embedded Linux-based mobile devices, co-author of multiple patents.
ALBA:	**Controls Engineer Intern**, Controls Section in 3rd Generation Synchrotron Light Facility
2008 - 2009 Spain	Software developer (C, C++) for the Storage Ring magnets' Power Supply controls, including porting of Linux device drivers (VME to PCI, 2.4 to 2.6) and implementing Tango Device Servers.
ISC Tech.:	**Development Engineer Intern**, World Rally Championship timing specialist company
2008 - 2008 UK	Responsible for a new generation of time measurement equipment, including real-time software for beam detectors (C for PIC microprocessors), electrical updates of prototypes and field tests.
CASPER:	**Technical Service Intern**, Leading computer manufacturer
2006 - 2006 Turkey	Successfully debugged and repaired a diverse range of computer defects.

Education

Ph.D.:	**Engineering and Technological Sciences in the discipline of Telecommunications**
2009 - 2017 Poland	Warsaw University of Technology, Faculty of Electronics and Information Technology Thesis: *Methods to Increase Reliability and Ensure Determinism in a White Rabbit Network* ⬀.
M.Sc.:	**Electronics & Computer Engineering with Cert. of Excellence**, *GPA* 4.65/5.00 (top 3%)
2004 - 2009 Poland	Warsaw University of Technology, Faculty of Electronics and Information Technology Thesis: *Universal Measurement System with Web Interface* ⬀ based on embedded Linux & FPGA.
B.Sc.:	**Informatics with Honours First Class**, *GPA* 81.75/100 (top 5%)
2007 - 2008 UK	Coventry University, Faculty of Engineering and Computing Thesis: *PSOnline – Primary School Online* ⬀ - a PHP-based Internet portal.

Professional Skills and Competencies

Leadership	Representation of CERN in IEEE, ITU-T, SNIA; chair in IEEE Working Group, team leader.
Coordination	Organisation of events at CERN with 50-100+ attendees: IEEE conf., IEEE meeting, workshops.
Management	Cross-domain projects with diverse stakeholders and users, including industry.
Communication	CERN guide, invited speaker, chair of meetings.
Editorial	Reviewer of 20+ articles for conferences, transactions, journals; guest editor in IEEE magazines.
FPGA HDL	VHDL, Verilog, SystemVerilog (RTL, simulation and verification).
Hardware	Review and supervision of PCB designs (schematics and layout).
Programming	C & C++ for desktop, embedded Linux, OS-less, real-time systems, Linux device drivers.
Scripting	Bash, Python, Matlab/Octave.
Networking	Development and operational experience with IEEE networking standards: 802.1, 802.3, 1588.
Synchronisation	Design of hardware, gateware, software, as well as standard development, modeling and testing.
EDA tools	ModelSim, ISE, Vivado, Vitis, Quartus, Altium, Matlab, Octave, LabView.
Testing	Professional Ethernet testers, environmental chambers, electromagnetic compatibility.
OS	Linux, embedded Linux, Windows (developer, support).
Doc.	LaTeX, Libre Office, MS Office, online collaborative tools.
Other	Version control (GIT, SVN), Tango control toolkit, Web Technologies (HTML, PHP, ASP).

Selected Courses

2022	Challenging Conversations
2020	Training on PCB design using Altium
2020	System on Chip Course with Reference Design
2018	Training on SystemVerilog for Verification Specialists with an introduction to UVM
2016	Structuring and Writing Reports, Effective Editing in English

Languages

Native	Polish
Foreign	English – Fluent	French – Intermediate

Extracurricular Activities

Associations	Erasmus Student Network (honorary member since 2011, active 2006 – 2011) International Assoc. for the Exchange of Students for Technical Experience (2005 – 2006)
Interests & activities	Travelling and photography enthusiast, squash league player, all-weather biker and runner, alpine skier, CERN guide and Open Days volunteer. Mechanical design and movie making in an all-open-source F*watch project ⬀.

Major Projects and Achievements

2021 – today **Frequency Scanning Interferometry** ⧉
Development of a cost-efficient and industry-scale system for the precise measurement of position of accelerator equipment, in the context of the High Luminosity LHC project.
Study of system requirements and operational principles of the underlying novel method to propose and implement a scalable, flexible and cost-effective architecture based on state-of-art off-the-shelf solutions, e.g., high-speed Ethernet, computation using Graphic Processing Units (GPUs). Leading a team of hardware, software, gateware developers through the full development cycle to provide acquisition electronics, in collaboration with BE-GM, and with tight deadlines.

2018 – 2022 **Guidelines for White Rabbit Infrastructure at CERN** ⧉
A project that defines generic architectural and operational guidelines for White Rabbit backbone infrastructure and attached systems. Deployed in all operational WR Networks at CERN.
The main initiator of the effort to ensure scalability, maintainability and availability of the White Rabbit infrastructure that distributes reference clock and timing signals to critical accelerator equipment. Responsibilities ranging from discussing concepts with different stakeholders, through developing and supervising implementations, to deploying in operation, documenting, iteratively adapting. The guidelines are used today at CERN and GSI.

2017 - 2018 **ISPCS 2018 conference at CERN** ⧉
ISPCS is an international IEEE symposium and plugfest, attended yearly by 100+ participants. Seeing through the organisation of the conference, from providing the idea to closing the 100+ kCHF budget. In many organisational aspects this conference had no precedent at CERN and thus required creative and tailored solutions. It involved cooperation with Knowledge Transfer, Legal, Logistics, Safety, Security, Visits, IT and Accommodation CERN services, external companies and partners, as well as timely interventions to solve a variety of emergencies.

2016 – 2021 **WR BTrain consolidation** ⧉
Update to use the White Rabbit technology for the mission-critical BTrain system that is indispensable to the operation of the LHC Injection Chain and the decelerators. Delivered on time. Coordination of efforts in TE-MSC, SY-EPC, SY-RF, SY-ABT and SY-BI groups, specification of common protocols and interfaces, and their implementation as shared VHDL IP cores. Integration of the IP cores into users' custom FPGA-based designs, code reviews and testing. Design, configuration and monitoring of deployed WR networks, support during commissioning and operation.

2012 – 2020 **WR Standardisation in IEEE 1588** ⧉
A strategic and successful effort to transform the CERN-born White Rabbit technology into an international IEEE 1588 standard, maximising its adoption by industry and ensuring its long-term support, in line with the Organization's interests. The standard was published in 2020.
Initiation of the effort, evaluation of an optimal and feasible path, promotion, lobbying for acceptance of WR's adaptation, sharing in-depth knowledge with world-leading experts. Leading a 4-year process for defining, negotiating and drafting a generic, industry-acceptable specification aligned with CERN needs, substantial contributions to a 3-year review process of 500+ pages.

Selected Publications and Presentations

EF@CERN:
2022
"Overview of relevant network protocols and standards" ⧉ – invited speaker at the Workshop on Ethernet Fieldbusses for Customs Electronics organised by CERN's Electronics Forum⧉, CERN;

OCP-TAP:
2021
"White Rabbit: An Accurate Time and Frequency Transfer over Ethernet Network" ⧉ – invited speaker for the Open Compute Project - Time Appliances Project⧉, online;

IEEE SA:
2020
"IEEE 1588-2019: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems" ⧉ – standard co-author;

ATFT:
2019
"White Rabbit" ⧉ – invited speaker at the BIPM Workshop on Advanced Time & Frequency Transfer ⧉, Sèvres, France;

IEEE802:
2013
"White Rabbit - Ethernet-based Solution for Sub-ns Synchronization and Deterministic, Reliable Data Delivery" ⧉ – invited tutorial speaker at IEEE802 Plenary Meeting, Geneva, Switzerland;

ISPCS:
2012
"Performance Results of the First White Rabbit Installation for CNGS Time Transfer" ⧉ – article main author, presented at the ISPCS conference, San Francisco, USA;

CERN:
2011
"White Rabbit Specification: Draft for Comments" ⧉ – document co-author, it defines the White Rabbit extension to the IEEE 1588 standard, published on ohwr.org.

ANNEX: List of Publications

Standards

IEEE SA: 2023	*"IEEE Std 1588g-2022: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems Amendment 2: Master-Slave Optional Alternative Terminology,"* ☑ vol., no., pp.1-14, 15 March 2023, doi: 10.1109/IEEESTD.2023.10070440.
IEEE SA: 2022	*"IEEE Std 1588b-2022: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems Amendment 1: Precision Time Protocol (PTP) Mapping for Transport over the Optical Transport Network (OTN),"* ☑ vol., no., pp.1-17, 16 Sept. 2022, doi: 10.1109/IEEESTD.2022.9895348.
IEEE SA: 2020	*"IEEE 1588-2019: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems,"* ☑ vol., no., pp.1-499, 16 June 2020, doi: 10.1109/IEEESTD.2020.9120376.

Journals and Magazines

IEEE-Com 2018	*"Trans-Industry Time Synchronization for a Smart Society,"* ☑ S. Ruffini, S. Rodrigues, M. Lipiński and M. Weiss, in IEEE Communications Magazine, vol. 58, no. 4, pp. 52-52, April 2020, doi: 10.1109/MCOM.2020.9071989.
IEEE-Com 2017	*"Synchronization standards toward 5G,"* ☑ S. Ruffini, S. Rodrigues, M. Lipiński and J. -C. Lin, in IEEE Communications Standards Magazine, vol. 1, no. 1, pp. 50-51, March 2017, doi: 10.1109/COMSTD.2017.7885238.
UFFC-T: 2018	*"WR Clock Synchronization: Ultimate Limits on Close-In Phase Noise and Short-Term Stability Due to FPGA Implementation,"* ☑ M. Rizzi, M. Lipiński, P. Ferrari, S. Rinaldi and A. Flammini, in IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 65, no. 9, pp. 1726-1737, Sept. 2018, doi: 10.1109/TUFFC.2018.2851842.
Elektronika: 2010	*"Uniwersalna platforma pomiarowa dla rozp. wirtualnego systemu pomiarowego (Distributed virtual measurement system),"* ☑ M. Lipiński, G. Kasprowicz, K. Pozniak, R. Romaniuk, in ELEKTRONIKA - KONSTRUKCJE TECHNOLOGIE ZASTOSOWANIA, 52. 89-93, January 2021, ISSN 0033-2089

Books

OWPW: 2016	*"Methods to Increase Reliability and Ensure Determinism in a White Rabbit Network,"* ☑ M. Lipinsk, Publisher OWPW, 2016, ISBN: 978-83-7814-590-5

Selected publicly available CERN documents

CERN: 2020	*"RoE structure-aware direct digital synthesis mapping using an OUI subType,"* ☑ J. Gill, M. Lipiński, 2020-01-17.
CERN: 2015	*"SyncE Characteristics of a White Rabbit Switch, Tests using Paragon-X, courtesy of Calnex,"* ☑ M. Lipiński, 2015-02-27
CERN: 2011	*"Discussion on a White Rabbit Based CERN Control and Timing Network,"* ☑ M. Lipiński, J-C. Bau, 2011-10.
CERN: 2011	*"White Rabbit Specification: Draft for Comments,"* ☑ E.G. Cota, M. Lipiński, T. Włostowski, E. van der Bij, J. Serrano, 2011-07-06.

Patents

US Patent: 2014	*"Mobile Device and Method for Controlling Messaging,"* ☑ Maciej Lipiński, Mikolaj Małecki, May 8, 2014, Network (717/171), Publication number: 20140130032, United States Patent and Trademark Office;
US Patent: 2014	*"Method and Apparatus for Sharing a File in P2P Systems,"* ☑ Marcin Goliszewski, Maciej Lipiński, Jan 2, 2014, Computer Conferencing (709/204), Publication number: 20140006511, United States Patent and Trademark Office;
US Patent: 2013	*"Mobile Device and Method for Controlling Messaging,"* ☑ Marcin Goliszewski, Maciej Lipiński, Dec 12, 2013, Auxiliary Data Signaling (e.g., Short Message Service (sms)) (455/466), Publication number: 20130331132, United States Patent and Trademark Office;

Conference Articles

ISPCS: 2018 — *"White Rabbit Applications and Enhancements,"* ☑, M. Lipiński et al., 2018 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), Geneva, Switzerland, 2018, pp. 1-7, doi: 10.1109/ISPCS.2018.8543072.

ISPCS: 2016 — *"White Rabbit Clock Characteristics,"* ☑, M. Rizzi, M. Lipiński et al., 2016 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), Stockholm, Sweden, 2016, pp. 1-6, doi: 10.1109/ISPCS.2016.7579514.

ISPCS: 2015 — *"Enhanced Synchronization Accuracy in IEEE 1588,"* ☑ O. Ronen and M. Lipiński, 2015 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), Beijing, China, 2015, pp. 76-81, doi: 10.1109/ISPCS.2015.7324687.

ICALEPCS: 2015 — *"Trigger and RF distribution using White Rabbit,"* ☑ T. Włostowski, J. Serrano, G. Daniluk, M. Lipiński, F. Vaga, 15th International Conference on Accelerator and Large Experimental Control Systems (ICALEPCS), Melbourne, Australia, 2015

ISPCS: 2014 — *""PPSi - A free software PTP implementation,"* ☑ P. Fezzardi, M. Lipiński, A. Rubini and A. Colosimo, 2014 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), Austin, TX, USA, 2014, pp. 71-76, doi: 10.1109/ISPCS.2014.6948694.

ICALEPCS: 2013 — *"White Rabbit Status And Prospects,"* ☑ J. Serrano, M. Cattin, E. Gousiou, E. van der Bij, T. Włostowski, G. Daniluk, M. Lipiński, D. Beck, J. Hoffmann, M. Kreider, C. Prados, S. Rauch, W.W. Terpstra, M. Zweig, 14th International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS), San Francisco, USA, 2013

TWEPP: 2013 — *"How to create successful open hardware projects - about White Rabbits and open fields,"* ☑ E. van der Bij, M. Arruat, M. Cattin, G. Daniluk, J.D. Gonzalez Cobas, E. Gousiou, J. Lewis, M.M. Lipiński, J. Serrano, T. Stana, N. Voumard, T. Włostowski, Topical Workshop on Electronics for Particle Physics (TWEPP), Perugia, Italy, 2013

IBIC2013: 2013 — *"The White Rabbit Project,"* ☑ J. Serrano, M. Cattin, E. Gousiou, E. van der Bij, T. Włostowski, G. Daniluk, M. Lipiński, 2nd International Beam Instrumentation Conference (IBIC), Oxford, UK, 2013

ISPCS: 2012 — *"Performance Results of the First White Rabbit Installation for CNGS Time Transfer,"* ☑ M. Lipiński et al., 2012 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication Proceedings, San Francisco, CA, USA, 2012, pp. 1-6, doi: 10.1109/ISPCS.2012.6336610.

ISPCS: 2012 — *"Distributed DDS in a White Rabbit Network: An IEEE 1588 Application,"* ☑ P. Moreira, J. Serrano, P. Alvarez, M. Lipiński, T. Włostowski, I. Darwazeh, 2012 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication Proceedings, San Francisco, CA, USA, 2012, pp. 1-6, doi: 10.1109/ISPCS.2012.6336611.

ICALEPCS: 2011 — *"Reliability in a White Rabbit Network,"* ☑ M. Lipiński, J. Serrano, T. Włostowski, C. Prados, International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS), Grenoble, France, 10 - 14 Oct 2011, pp.698-701.

ISPCS: 2011 — *"White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization,"* ☑ M. Lipiński, T. Włostowski, J. Serrano and P. Alvarez, 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication, Munich, Germany, 2011, pp. 25-30, doi: 10.1109/ISPCS.2011.6070148.

PAC: 2011 — *"Accelerator Timing Systems Overview,"* ☑, J. Serrano, P. Alvarez, M. Lipiński, T. Włostowski, Particle Accelerator Conference, New York, USA; April 2011

SPIE: 2010 — *"Virtual measurement system,"* ☑ M. Lipiński, K. Pozniak; IEEE-SPIE on Photonics and Web Engineering, SPIE, 2010, 1-4; February 2010, Wilga, Poland.

SPIE: 2009 — *"Universal Measurement System with Web Interface,"* ☑ M. Lipiński, G. Kasprowicz, Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2009; Proc.SPIE vol.7502, ISSN 0277-786X, ISBN 978-0-8194-7813-9; July 2009

ICALEPCS: 2009 — *"PCI/cPCI Interface for PSI Power Supply Controller,"* ☑ D. Beltran, F. Becheri, D. Fernandez-Carreiras, J.V. Gigante, J. Klora, L. Krause, M. Lipiński, International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS), Kobe, Japan, 12 - 16 Oct 2009.